DESIGN, DEVELOPMENT, FABRICATION AND DELIVERY of PROTOTYPE SILICON MONOLITHIC AMPLIFIERS

Final Report

Report No. 08863-6001-T0-00 25 July 1969

Prepared for

National Aeronautics and Space Administration
George C. Marshall Space Flight Center

Huntsville, Alabama

Contract No. NAS8-20732

TRW

Systems Group

DESIGN, DEVELOPMENT, FABRICATION AND DELIVERY
of
PROTOTYPE SILICON MONOLITHIC AMPLIFIERS

Final Report

Report No. 08863-6001-T0-00

25 July 1969

Prepared for

National Aeronautics and Space Administration
George C. Marshall Space Flight Center

Huntsville, Alabama

Contract No. NAS8-20732

TRW

Systems Group

FOREWORD

This work was performed by the Microelectronics Center of TRW Systems Group, TRW Inc., One Space Park, Redondo Beach, California, under NASA Contract No. NAS8-20732, "Design, Development, Fabrication and Delivery of Prototype Silicon Monolithic Amplifiers." This report covers work conducted from June, 1967 through July, 1969 and is identified as Report No. 08863-6001-T0-00 by the Contractor. Members of the Technical Staff include D. R. Breuer, Project and Design Engineer, and J. L. Buie, Head, Microelectronics Research and Development Section.

CONTENTS

CONTENTS (Continued)

ILLUSTRATIONS

ILLUSTRATIONS (Continued)

ILLUSTRATIONS (Continued)

TABLES

1.0 INTRODUCTION

This report describes the work performed under contract NAS8-20732 to develop a monolithic differential operational amplifier to be used in control system electronics for space vehicles. The electrical specifications emphasize large output voltage swing, high open loop gain, low input dc errors, and low power dissipation. Specifically, they are:

(1) Type: Differential Operational Amplifier. (See Figure 1-1.)

(2) Drift: Maximum output drift of 15 mV over the temperature range of -55°C to +125°C with: $R_{in1} = R_{in2} = 50$ K ohm, $R_{f1} = R_{f2} = 500$ K ohms, and the input shorted. (Scaling resistors external to oven.) See Figure 1-1.

(3) Power Consumption: Quiescent condition 0.050 watt.

(4) Output Voltage Swing: 60 volts peak-to-peak with $\pm$ 6 mA output current.

(5) Output Impedance: (Same conditions given under drift specifications.) Less than 100 ohms over the linear range of 0 to $\pm$ 30 volts with load variations from 5 K to no load.

(6) Power Source: $V_{cc} \pm 5\%$, sufficient to meet output voltage swing and power dissipation.

(7) Phase Shift: Not more than 1.5 degrees lag at 5 Hz, $R_f = 500$ K.

(8) Open Loop Voltage Gain: Minimum of 10^6.

(9) Gain with External Scaling Resistors: Approximately 10.

(10) Common Mode Rejection: Minimum 60 dB.

(11) Frequency Response: Maximum of 3 dB down at 2 KHz closed loop.

The initial phase of this contract was directed toward the design and fabrication of a monolithic amplifier incorporating vertical NPN and vertical PNP transistor structures formed in a dielectrically isolated substrate. (See Appendix A.) Due to the low yield of this technology, the final phase was redirected toward dielectrically isolated vertical NPN and lateral (or side injection) PNP transistors. This processing

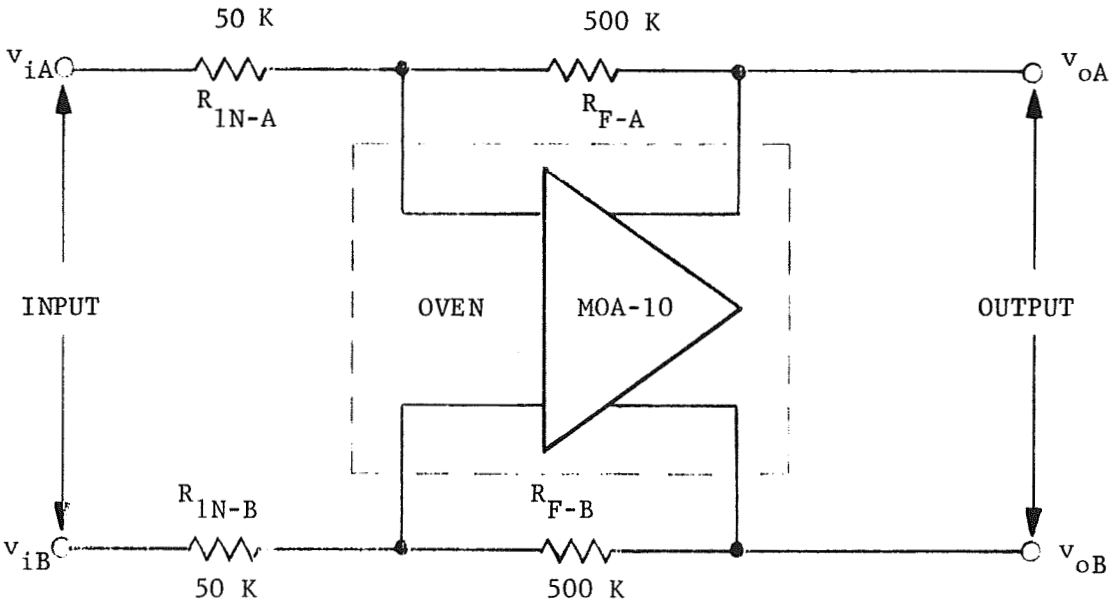

Figure 1.1. Closed Loop Feedback Connection (Gain of 10)

coupled with thin-film resistors, has been demonstrated capable of producing amplifiers with reasonable yield. Figure 1-2 shows a photograph of the final amplifier configuration, mounted in a sealed transparent-covered package.

This report includes data on the processing technology, circuit design, integrated circuit layout, testing, and evaluation of this amplifier.

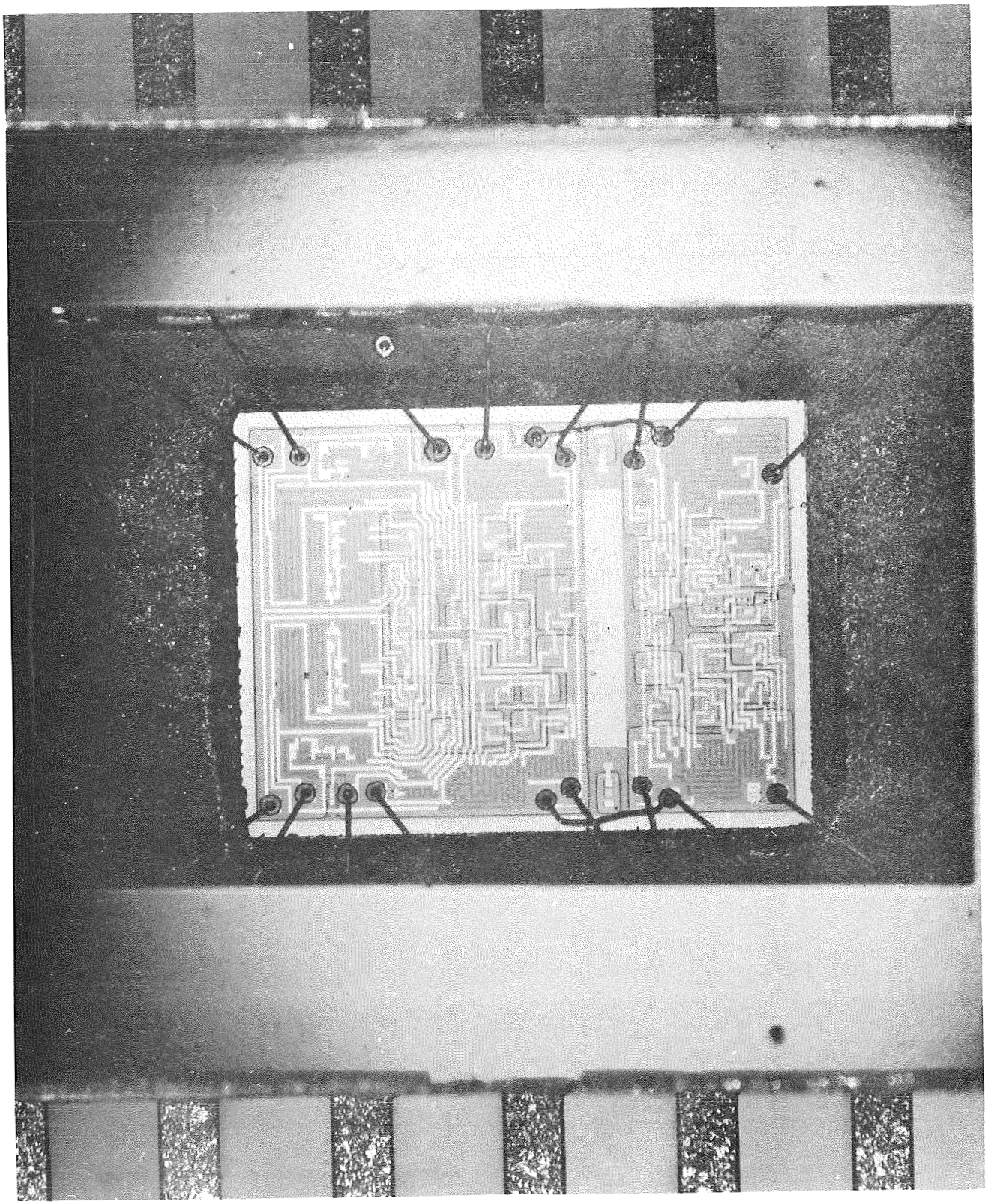

Figure 1.2 MOA-10

2.0 CIRCUIT ORGANIZATION

2.1 General Description

The MOA-10* amplifier, shown schematically in Figure 2-1, is composed of the following four voltage gain stages:

First: Q_1 and Q_2 is an inverting common-emitter input stage (used also for drift** compensation),

Second: Q_3 and Q_4 is a unity gain, inverting common-emitter stage (used for offset*** compensation)

Third: Q_{5A}-Q_{6A} and Q_{5B}-Q_{6B} is a noninverting common collector-common base stage, and

Fourth: Q_{26} and Q_{27} is an inverting common-emitter stage.

Collectively, these stages offer an overall voltage gain in excess of 1.0×10^6. A unity gain, inverting stage, Q_3 and Q_4, is required to provide the proper phase relationship for negative common-mode feedback when the external feedback resistors are connected as shown in Figure 1-1. Note that the differential feedback phase is a matter of choice in connecting the external resistors; however, the correct common-mode feedback phase must be supplied by the amplifier and cannot be reversed by external interconnections. Unity gain stage, Q_3 and Q_4, is also used for dc zero offset compensation.

---

*MOA-10 represents Monolithic Operational Amplifier - Number 10 (or fabricated on substrate type number 10).

**Drift refers to the dc output voltage as a function of temperature with the inputs shorted.

***Offset refers to the dc output voltage with the inputs shorted at a constant (for instance, room) temperature.

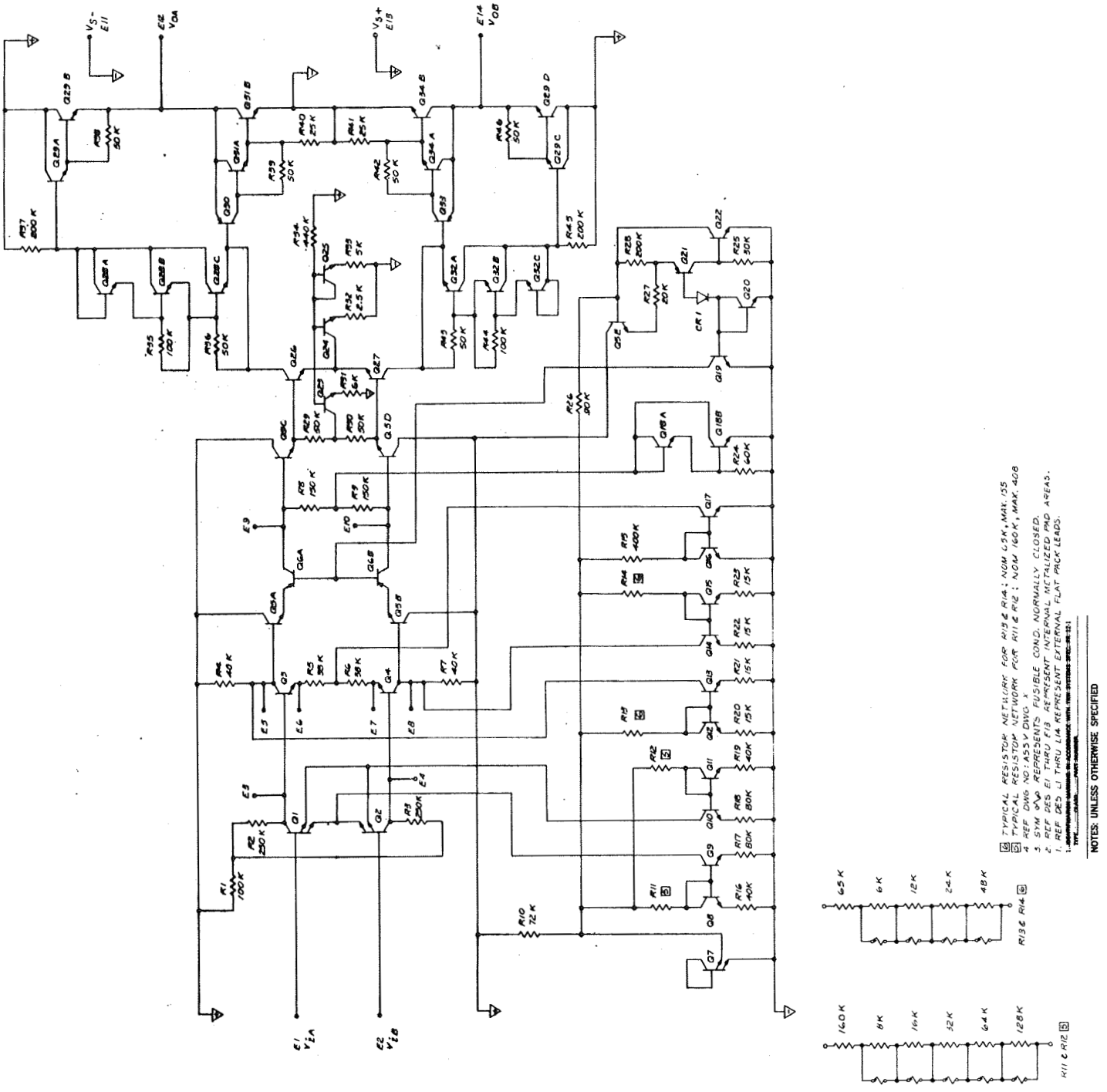

Figure 2.1 MOA-10 Schematic

A voltage regulator is formed by R_{10} and Q_7 to stabilize the currents generated by Q_8 through Q_{17} against variations in the power supply voltage. Each current generator includes a diode connected transistor for temperature stabilization and emitter resistors for reducing the effect of V_{BE} unbalances. Transistors Q_9 and Q_{10} deliver current into the dual emitter input stage (see Section 2.4 on drift control) and Q_{13} and Q_{14} deliver current into R_4 and R_7 for offset control. Transistor Q_{17} supplies common-mode current for Q_3 and Q_4.

The noninverting gainstage is biased by controlling the base currents of the Q_{6A} and Q_{6B} common-base stage. Since side-injection PNP transistors are used, with Betas ranging from 1 to 10, the common-mode current generator must be designed to compensate for this Beta range and thereby stabilize the common-mode voltage across R_8 and R_9. Components Q_{19}, Q_{20}, Q_{21}, CR1, R_{25}, R_{26}, R_{27}, and R_{28} provide this compensated current. The emitter base voltage of Q_{22} controls the current through R_{25} and therefore Q_{21}. If the Betas of Q_{21} and Q_{6A}-Q_{6B} are approximately equal, and the current out of Q_{19} is approximately equal to the current into Q_{20}, the collector currents of Q_{6A} and Q_{6B} become directly dependent on the voltage across R_{25}, regardless of PNP Betas. Components R_{26}, R_{27}, and Q_{5E} form a local feedback loop for establishing I_{C21} equal to $V_{BE\text{-}22}/R_{25}$.

Transistors Q_{18A} and Q_{18B} provide a double diode drop to sink currents from R_8 and R_9. These diode drops compensate the emitter base voltages of Q_{5C}-Q_{26} and Q_{5D}- Q_{27}, thereby aiding in maintaining a sufficient voltage across the current generator formed by Q_{24}.

The output Class B current drive stage is formed by positive current composite Q_{29A} and Q_{29B}, and negative current composite Q_{30}, Q_{31A}, and Q_{31B}. Diode connected transistors Q_{28A}, Q_{28B}, and Q_{28C} compensate for the emitter base voltages of Q_{29A}, Q_{29B}, and Q_{30} to reduce the dead zone from 2.0 volts to a few millivolts, etc.

2.2 Power Dissipation

The specification for maximum power dissipation of 50 mW necessitates operating each transistor at a low current level. Table 2.1 lists the nominal current values, which add up to a total current of 0.92 mA from a 45 volt power supply. This produces a quiescent power consumption of

$$P_D = (45 \text{ volts}) \times (0.92 \text{ mA}) = 41 \text{ milliwatts} \qquad (2.1)$$

TABLE 2.1

AMPLIFIER BIAS LEVELS

Each Component	Nominal Current Level*
Q_1 and Q_2	20 to 10μa **
Q_3 and Q_4	10μa
Q_{5A}, Q_{6A} and Q_{5B} , Q_{6B}	10μa
Q_{5C} and Q_{5D}	40μa
Q_{26} and Q_{27}	100μa
Q_{29A} and Q_{29C}	12μa
R_{40} and R_{41}	24μa
R_{10}	500μa
R_{34}	100μa

* Assuming nominal resistance values

** Value is dependent on drift adjustment (see Section 2.4)

The design will therefore accommodate resistor absolute values of 80 percent of nominal value and still meet the quiescent power specification.

2.3 Open Loop Gain

The open loop voltage gain of the MOA·10 can be represented by the following equation.

$$A_{vo} = A_1 \times A_2 \times A_3 \times K_1 \times A_4 \times K_2 \tag{2.2}$$

where

$$A_{vo} \equiv \text{overall voltage gain at dc} \tag{2.3}$$

$$A_1 \equiv \text{voltage gain of input stage, } Q_1 \text{ and } Q_2 \tag{2.4}$$

$$A_2 \equiv \text{voltage gain of 2nd stage, } Q_3 \text{ and } Q_4 \tag{2.5}$$

$$A_3 \equiv \text{voltage gain of 3rd stage, } Q_{5A}\text{-}Q_{6A} \text{ and } Q_{5B}\text{-}Q_{6B} \tag{2.6}$$

$$K_1 \equiv \text{voltage gain (attenuation) of emitter followers } Q_{5C} \text{ and } Q_{5D}. \tag{2.7}$$

$$A_4 \equiv \text{voltage gain of 4th stage, } Q_{26} \text{ and } Q_{27} \tag{2.8}$$

$$K_2 \equiv \text{voltage gain (attenuation) of output emitter follower composite} \tag{2.9}$$

Each component can be approximated as follows:

$$A_1 = \frac{R_2 \| h_{oe_1}^{-1} \| (\beta_3)(r_{E3} + R_5)}{r_{E_1} + r'_{E_1} + \frac{R_s + r'_{\beta 1}}{\beta_1}} \tag{2.10}$$

$$A_2 = \frac{R_4 \| h_{oe_3}^{-1} \| (\beta_{5A}) \left(r_{E5A} + r_{E6A} + \frac{r'_{B\ 6A}}{\beta_{6A}} \right)}{R_5 + r_{E3} + r'_{E3}} \tag{2.11}$$

$$A_3 = \frac{R_8 \| h_{oe_6}^{-1} \| (\beta_{5C}) (r_{E5C} + R_{29} \| \beta_{26} r_{E26})}{r_{E5A} + r_{E6A} + \frac{r'_{B\ 6A}}{\beta_{6A}}} \tag{2.12}$$

$$K_1 = \frac{(R_{29} \| \beta_{26} r_{E26})}{(R_{29} \| \beta_{26} r_{E26}) + r_{E5C}} \tag{2.13}$$

$$A_4 \doteq \frac{R_{37} \| h_{oe_{26}}^{-1} \| (\beta_{29A}) (r_{E29} + \beta_{29B} R_L + R_{38} \| \beta_{29} r_{E29})}{r_{E26} + r'_{E26}} \tag{2.14}$$

$$K_2 \doteq \frac{R_{38} \| \beta_{29_B} r_{E29_B} + \beta_{29B} R_L}{r_{29A} + R_{38} \| \beta_{29_B} r_{E29_B} + \beta_{29B} R_L} \times \frac{R_L}{R_L + r_{E29B} + \frac{r_{E29A} + R_{37} \beta_{29A}}{\beta_{29B}}} \tag{2.15}$$

where

$$r_E = \frac{KT}{qI_E} , \tag{2.16}$$

$r'_E \equiv$ emitter parasitic resistance, (2.17)

$r'_B =$ base spreading resistance, (2.18)

$$
\begin{array}{llll}
\beta_3 = 70 & R_s = 50K & h_{oe_1}^{-1} = 3 \times 10^6 & r_{E5A} = 2600 \\
\beta_{5A} = 70 & R_2 = 250K & h_{oe_3}^{-1} = 5 \times 10^6 & r_{E6A} = 2600 \\
\beta_{6A} = 3 & R_5 = 38K & h_{oe_6}^{-1} = 5 \times 10^6 & r'_{B1} = 70 \\
\beta_{5C} = 70 & R_4 = 40K & h_{oe_{26}}^{-1} = 5 \times 10^5 & r'_{B6A} = 100 \\
\beta_{26} = 70 & R_8 = 150K & r_{E1} = 1300 & r_{E5C} = 650 \\
\beta_{29A} = 70 & R_{29} = 50K & r_{E3} = 2600 & r_{E26} = 260 \\
\beta_{29B} = 70 & R_{37} = 200K & r'_{E1} = 5 & r_{E29A} = 2200 \\
 & R_L = \frac{5K}{2} = 2.5K & r'_{E3} = 5 & r'_{E26} = 5 \\
 & & & r_{E29B} = 10
\end{array}
\qquad (2.19)
$$

The output is assumed positive and in the middle of the dynamic range. The amplifier input-output transfer function changes as the output voltage traverses from positive to negative. The effect on dc gain is assumed to be negligible. The normal gain values become:

$$A_1 = 106$$

$$A_2 = 0.89$$

$$A_3 = 24.2$$

$$K_1 = 0.955$$

$$A_4 = 527$$

$$K_2 = 0.96$$

$$A_{VO} = 1.1 \times 10^6$$

The gain is heavily dependent upon temperature (Eq. 2.16) and Beta, and is lightly dependent upon resistor absolute values and collector dynamic impedances.

2.4 DC Zero Compensation

The drift specification is recognized as the most challenging design objective. Figure 2.2 aids in illustrating this specification.

A strict interpretation of the contract specifications would identify the zero voltage line as any nominal dc differential output voltage. Or, in other words, the ±15 mv error range applies only to temperature drift and not to nominal differential offset voltage.

However, a more demanding interpretation, of including the nominal differential offset voltage in the ±15 mv error range, makes the amplifier more adaptable to high performance applications, and is therefore considered a design goal.

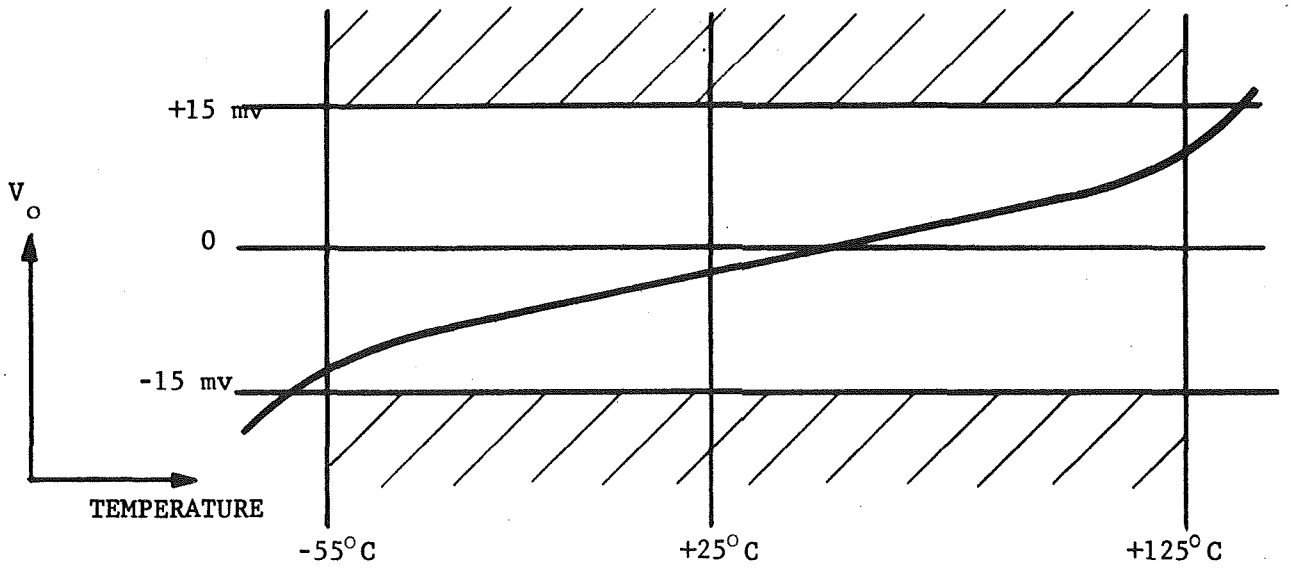

Figure 2.2. Typical Output Voltage Characteristic vs. Temperature

The total output offset error includes the following principal components.

V_1 ≡ due to the difference of the emitter-base voltages of the first stage

V_2 ≡ due to the difference of the input base currents of the first stage

V_3 ≡ due to the unbalance of the collector load impedance of the first stage

V_4 ≡ due to the difference of the collector-base leakage currents of the input stage

V_5 ≡ due to the difference of the input base currents of the second stage

V_6 ≡ due to the difference of the emitter-base voltages of the second stage

V_7 ≡ due to the unbalance in the feedback resistors which create offsets due to the amplifier input currents

The accumulation of all of these components, with no means of compensation, would impose a severe yield loss on the monolithic amplifier if the ±15 mv output specification must be met (±1.5 mv referred to the input). A technique of compensating for the inherent amplifier offset and temperature drift has therefore been incorporated. The design of the amplifier is directed toward minimizing the nonlinear drift terms, namely those due to transistor base and leakage currents, with the compensating circuitry correcting for the linear terms.

The most troublesome component in the list of offset errors is V_2. The feedback impedance is 500k ohms, so V_2 is typically dominant. ·· at lower temperatures. For instance, the input stage is designed to operate at collector currents from 20 to 10μa. With transistor Betas of 100 and 10% matching, the 20 μa differential input current offset will create a 10 mv error at the output. At -55°C this error is doubled.

The compensation scheme operates on an input stage V_{BE} mechanism. While this technique is effective in compensating all accumulated drift components, it is required to work the hardest at lower temperatures due to input stage base current errors. Therefore the largest errors are expected at lower temperatures.

It can be seen that drift compensation is accomplished by controlling the relationship of the common-mode currents delivered to the double emitter input transistors (see reference 1). This is shown

---

[1] Gary L. Baldwin and Graham A. Rigby, "New Techniques for Drift Compensation in Integrated Differential Amplifiers", IEEE Journal of Solid State Circuits, vol. SC3, No. 4, Dec. 1968.

in Figure 2.3 in which two pairs of transistors are connected in parallel. The emitter base area of Q_{1A} is made larger than Q_{1B} so that changing the common-mode current, I_1 modifies the temperature drift and offset introduced by that pair. Transistor Q_{2B} emitter-base area is made the same as Q_{1A} and Q_{2A} like Q_{1B} so that each pair neutralizes the drift, offset unbalance of the other pair. By adjusting I_1 and/or I_2, accumulated drift, offset errors can be compensated, and a minimum drift condition can be obtained without causing severe circuit unbalances which deteriorate the common-mode rejection and power supply rejection performance. Note that Q_{1A} and Q_{2A} of Figure 2.3 can be coalesced structures with one collector, one base, and two emitters. The circuit can then be redrawn as Q_1 and Q_2 in Figure 2.1. Adjustments of I_1 and I_2 are accomplished by laser pulsing R_{11} and/or R_{12}. Large incremental changes are made by blowing out metal fuse links.

After the temperature drift has been minimized, the residual offset is compensated by introducing differential currents into the second stage collector resistors, R_4 and R_7. If the input stage gain is high and relatively constant with temperature, the resultant change in drift is maintained small. Offset adjustment is accomplished by laser pulsing R_{13} and/or R_{14}, with large incremental changes made by blowing out metal fuse links.

2.5 Common-Mode Rejection and Power Supply Rejection

The primary cause for reduced common-mode rejection is due to unbalances in the input stage. The drift correction technique introduces a negligible unbalance in the differential signal path. It is reported (reference 1) that for a ratio of 20:1 in the two common-mode currents

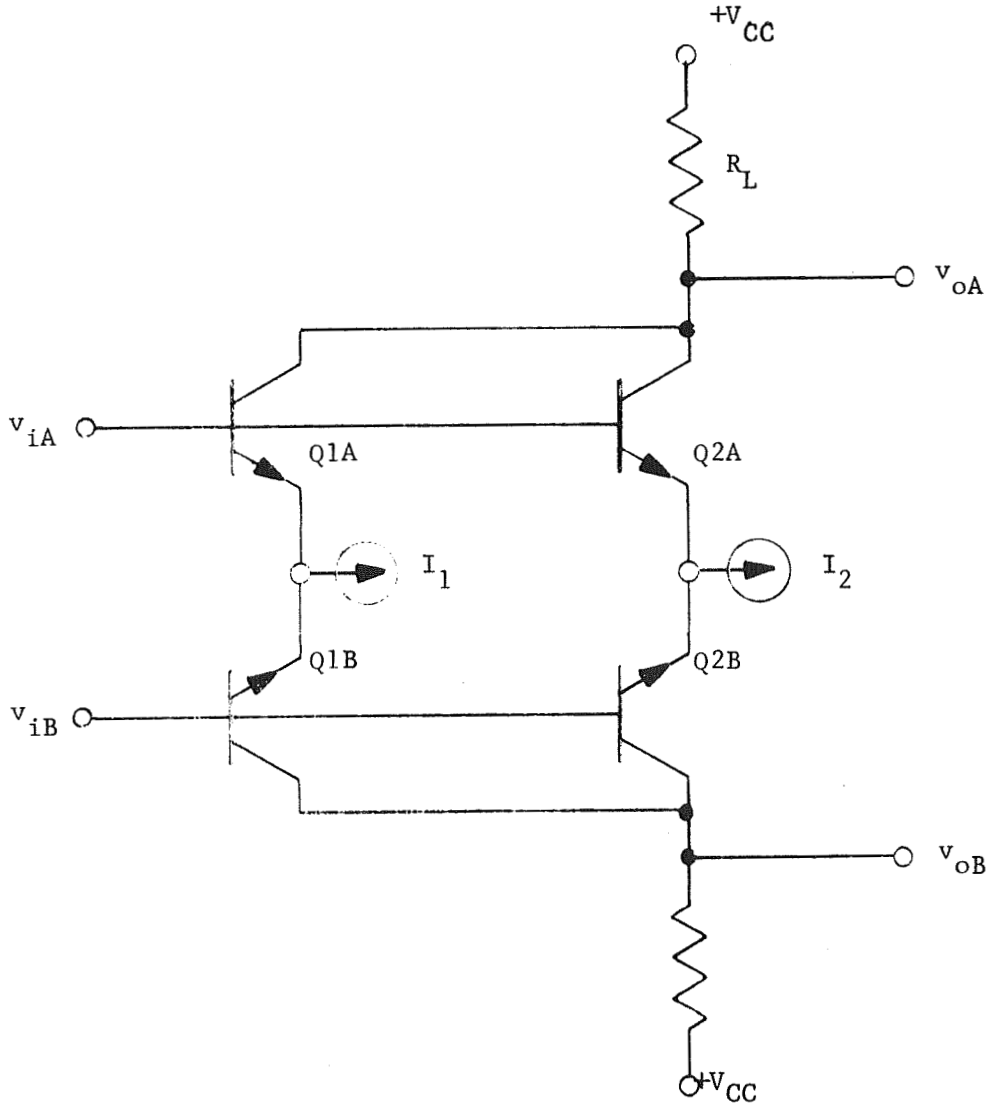

Figure 2.3. Input Stage Drift Compensation

of the input stage (say Q_9 delivering 10μa and Q_{10} delivering 2 ma) the common-mode rejection factor is reduced by only 5db. Since in practice the common-mode current ratios would never exceed 2:1, this effect on common-mode rejection performance is not important.

The adjustment procedure for drift-offset compensation is preceded by laser trimming R_2 and R_3 for an equality between 0.1 to 1.0%. This step contributes to high common-mode rejection factors. As the input common-mode voltage is changed, the finite collector dynamic output impedance of Q_9 and Q_{10} create a corresponding change in the common-mode collector currents of Q_1 and Q_2. This in turn creates a differential signal due to impedance unbalances at the collectors of Q_1 and Q_2. The common-mode rejection due to this effect is given by

$$\text{CMR} \equiv \frac{\text{Differential input to differential output gain}}{\text{Common-mode input to differential out gain}} \tag{2.20}$$

$$= \frac{10}{\dfrac{(R_2 - R_3)}{h_{oe}^{-1}(Q9 \,||\, Q10)} \times \dfrac{10}{A_1}} \tag{2.21}$$

for a one volt common-mode input voltage change, where

$h_{oe}^{-1}(Q9 \,||\, Q10)$ ≡ parallel output dynamic impedance of Q9 and Q10

A_1 ≡ given by equation 2.10

$(R_2 - R_3)$ ≡ differential in collector resistance, must include unbalances due to $h_{oe_1}^{-1}$ and $h_{oe_2}^{-1}$, etc

The CMR ratio becomes

$$\text{CMR} \leq \frac{\left(h_{oe}^{-1}(Q9 \;\; Q10)\right) \times A_1}{(R_2 - R_3)} \tag{2.22}$$

$$= \frac{(10^6 \text{ ohms}) \times 106}{2.5 \times 10^3} \simeq 4 \times 10^4 \tag{2.23}$$

or 92 db for an effective 1% match in R_2 and R_3. The common-mode input voltage range design value is over 30 volts.

The power supply rejection should also be high since the bias currents of the input stage are regulated by R_{10} and Q_7. It can likewise be shown that due to a similar argument as above,

$$PSR \equiv \frac{\text{Power supply voltage change}}{\text{Equivalent input voltage change}} \tag{2.24}$$

$$= \frac{\Delta V_s}{\frac{\Delta V_s}{V_s} \times I_{CM} \times K_R \times \frac{(R_2 - R_3)}{A_1}} \tag{2.25}$$

$$= \frac{A_1 V_s}{I_{CM} K_R (R_2 - R_3)} \tag{2.26}$$

or 73 db for an effective 1% match in R_2 and R_3, with

$$I_{CM} \equiv \frac{I_{C1} + I_{C2}}{2}, \text{ and} \tag{2.28}$$

$$K_R \equiv \text{Regulation factor of zener voltage regulation}$$
$$\geq 20 \tag{2.29}$$

2.6 Output Voltage Swing

The 60 volt peak-to-peak differential output voltage swing specification requires each output to swing linearly at least $\pm$15 volts about its quiescent value (the output common-mode voltage). Care must be exercised in the circuit design to insure that this specification can be met. The worst case minimum power supply voltage can be calculated by summing the following items:

Output voltage swing ΔV_o	= 30 volts
Most positive voltage of Q_{26} - Q_{27} emitters	= 5 volts
Current loading $R_{37} \times I_L/(\beta_{29A}\beta_{29B})$	= 1 volt

NPN V_{BE} voltages	= 1.8 volts
PNP V_{BE} voltages	= 2.7 volts
Output common-mode voltage accuracy	= 2.5 volts
$\underline{V_S}$ ≡ Minimum (worst case) supply voltage	= 43 volts

The $I_C V_C'$ drop in the emitter follower collectors does not contribute to a loss in output swing unless they exceed the combined components due to V_{BE} and current loading. With V_C' valves ≤ 300 ohms and I_C ≤ 7 ma, this term is unimportant.

2.7 Closed Loop Stability, Frequency Response, Phase Shift, Slewing Rate, and Noise

These specifications must be considered simultaneously to obtain a properly designed roll-off network for the MOA-10. Closed loop stability requires a controlled phase-gain characteristic of the loop gain function through unity gain. Conflicting requirements are imposed upon the placement of the dominant pole in the frequency domain and the electrical location of the dominant pole in the circuit.

Maximum stability margins are obtained by placing the dominant pole at a low frequency, while frequency response and slewing rate specifications prefer a high frequency controlling pole. A compromise is obtained by using a rate of roll-off of the loop gain response which approaches 9 db/octave.

If the dominant pole is placed at the input stage, the noise becomes excessive. This is due to the high frequency shorting nature of a low frequency pole, which essentially opens the feedback loop at high frequencies. This can be seen in Figure 2.4. The high frequency noise which is generated at the input of A_2 is amplified by $A_2 \times A_3 \times A_3$, there-

fore producing a large noise at the output. This technique is therefore unacceptable.

If the dominant pole is placed at the output stage, which removes the noise problem, a slewing problem arises, since the voltage swing is greatest at the output. A compromise solution is appropriate.

The assumed requirement for output noise is that it be less than 10 millivolts. Likewise compatible with other contractual specifications, the goal for slewing rate is that it be sufficiently high to pass a 60 volt, 2 KHz sine wave undistorted.

One possible solution is presented in Figure 2.5 which creates pole-zero combinations represented in the Bode diagram of Figure 2.6. This has been successfully demonstrated with the integrated circuit.

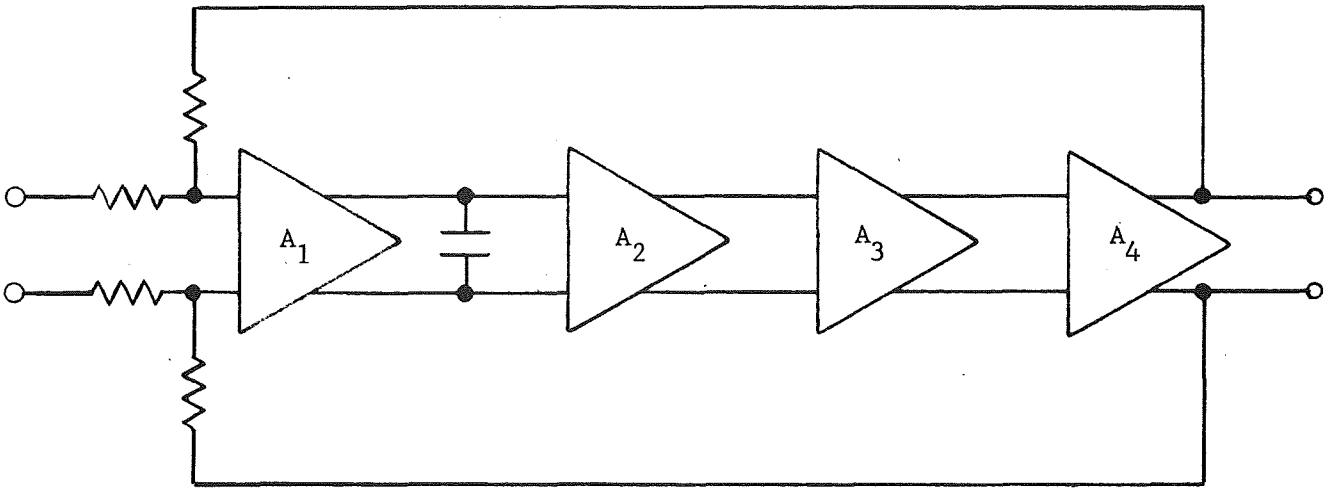

Figure 2.4. Roll-off Configuration Which Creates Excessive Noise

2.8 Output Impedance

The closed loop output impedance, which is specified to be less than 100 ohms, is approximately the open loop output impedance divided by the loop gain. The resistive component of the open loop output impedance is, to a first order approximation.

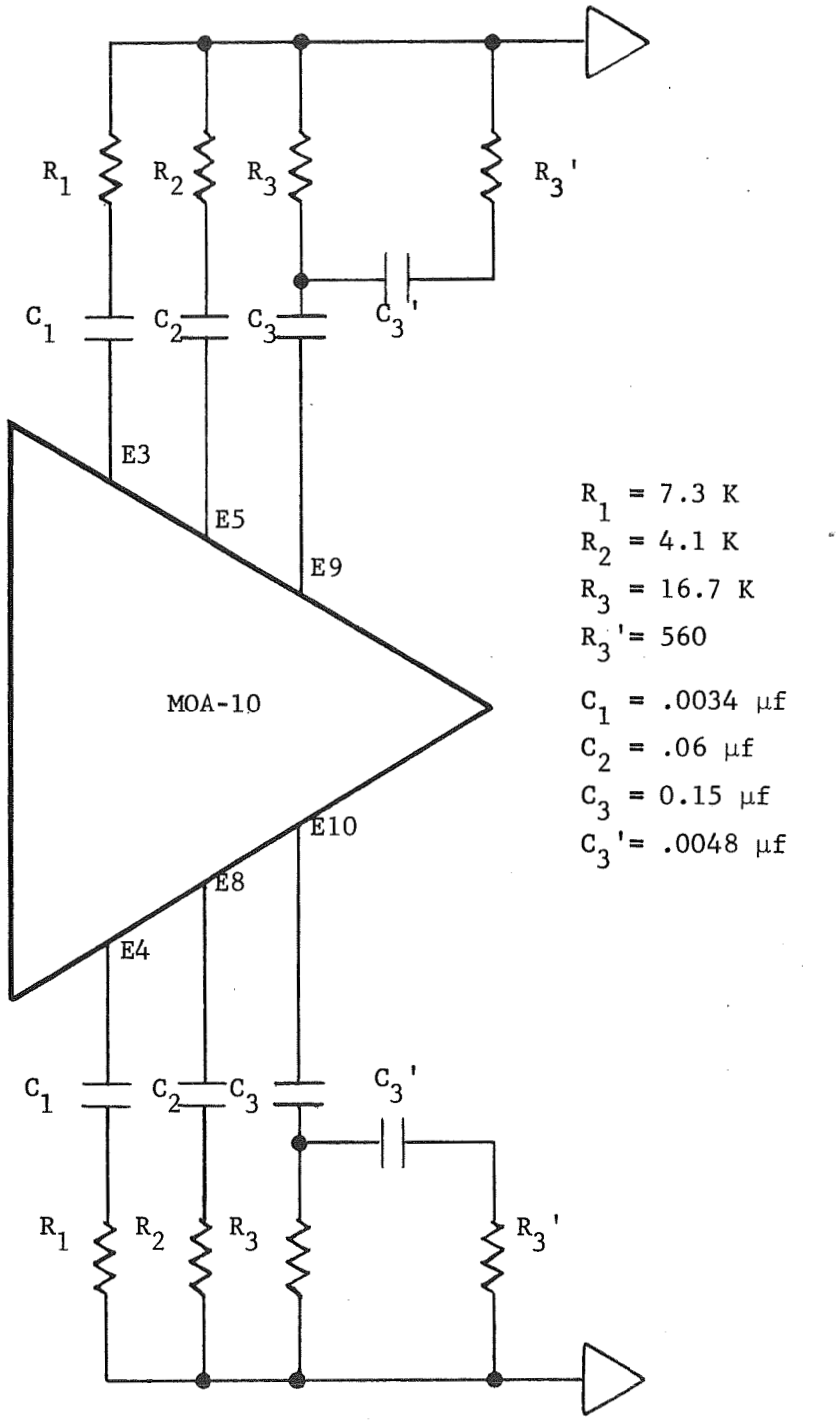

Figure 2.5. A Possible Roll-off Network for Stabilization

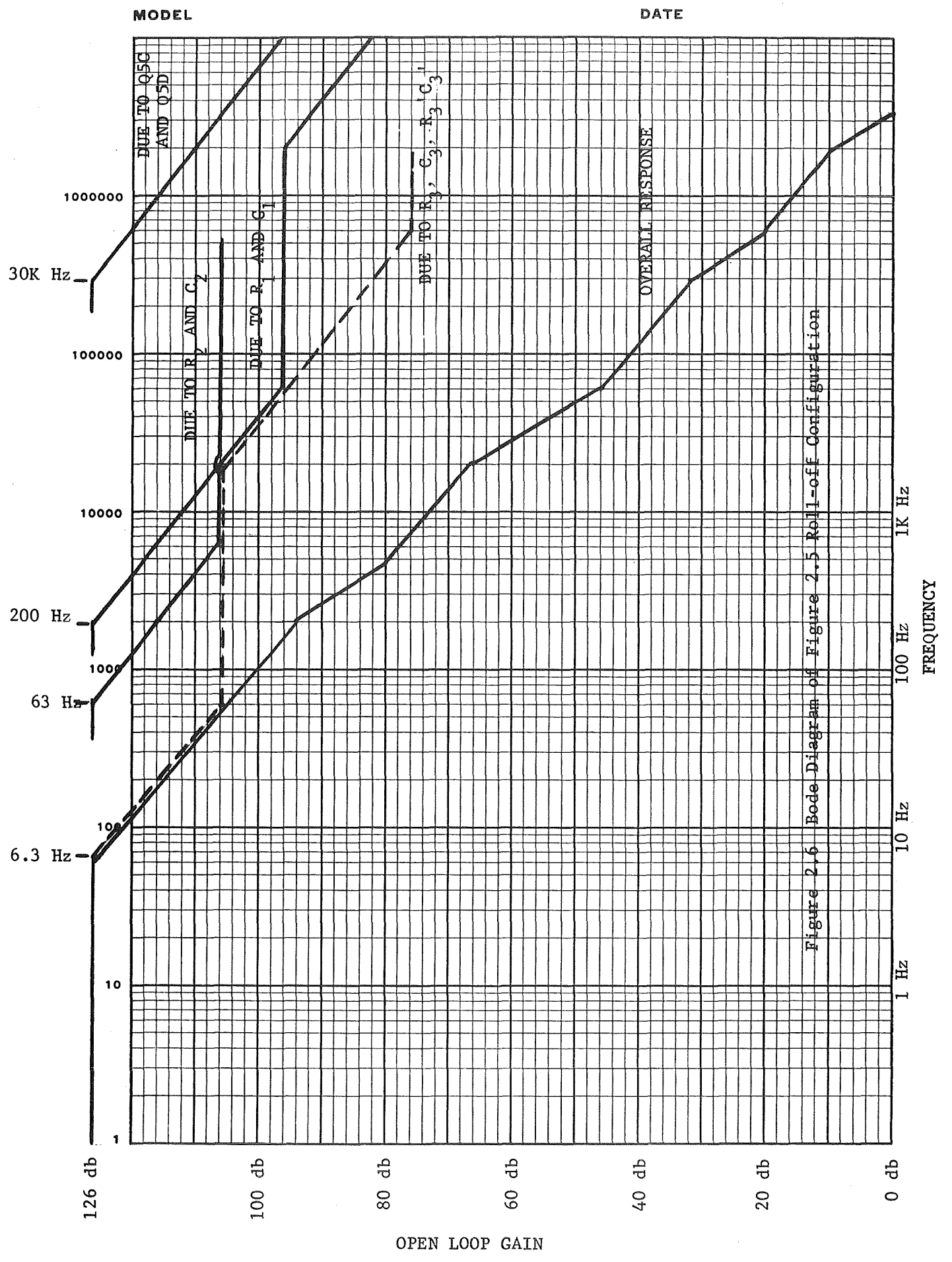

Figure 2.6 Bode Diagram of Figure 2.5 Roll-off Configuration

$$R_o' = \frac{200K}{\beta^*} \quad , \tag{2.30}$$

where

$$\beta^* \equiv \text{composite current gain of output, emitter followers} \tag{2.31}$$

$$R_o' \equiv \text{open loop output resistance,} \tag{2.32}$$

so that

$$R_o = \frac{R_o'}{T} = \frac{1}{T} \times \frac{200K}{\beta^*}, \tag{2.33}$$

where

$$T \equiv \text{loop gain} \tag{2.34}$$

The current gain, β^*, is established by different devices for positive and negative outputs, however for either

$$\beta^* > 2500 \tag{2.35}$$

This makes

$R_o' < 80$ ohms, and if

$T \geq 10^5$, R_o becomes very much smaller than 100 ohms.

Since the output drive circuit is Class B, there is a small voltage range about zero in which the loop gain drops to zero, and the output impedance increases. This is inherent to this type of circuitry and cannot be easily avoided without increasing the power dissipation.

The measurement of output impedance must not be confused with thermal feedback effects. When a large output voltage is maintained, the input stage may develop thermal differentials which appear as an input voltage. This effect can be minimized by measuring the electrical output resistance with an ac signal.

3.0 INTEGRATED CIRCUIT TECHNOLOGY AND DESIGN

The electrical specifications of this operational amplifier impose significant demands on the technologies required to fabricate the circuit. For instance, the combined specifications of 60-volt peak-to-peak linear output voltage swing and 50 mW maximum power dissipation are best accommodated with a dielectrically isolated NPN-PNP complementary monolithic circuit incorporating high sheet resistance (2000 ohms per square) thin film cermet resistors. These advanced technologies are being used and combined for the first time in this operational amplifier.

The circuit statistics include:

97 Devices*

50 Transistors**

34 Isolated Transistor Structures***

47 Resistors

4.4 Megohms Total Resistance

3.1 Processing

The substrate processing followed the sequence of Figure 3-1, with the processing data recorded on the form of Figure 3-2. The surface processing and data sheet is shown in Figure 3-3.

Dielectric isolation was chosen for the following reasons:

1) Due to the elimination of substrate dc parasitics, the complementary transistors are more easily fabricated in this type of substrate

---

* A device means either a transistor or a resistor.
** Counting separate base areas.
*** Some of these isolated collector regions include more than one base region.

MOA10 PROCESSING

DEVICE CHARACTERISTICS:

NPN: Beta = 160 at +25°C at 5 mA
$BV_{CEO} \geq 40$ volts (implying BV_{CBO} = 120 volts)

PNP: Beta = 1-10 at +25°C at 100μA
$BV_{CEO} \geq 40$ volts (implying BV_{CBO} = 120 volts

SUBSTRATE PARAMETERS:

1. Starting Material: N-type, 3 ohm-cm
2. $W_B = 3.6$; $R_{BS} = 150$ ohms/square after redistribution.
3. $W_E = 2.5$; $R_{ES} = 2.5$ ohms/square
4. Nominal isolation etch depth = 30μ (± 5μ tolerance) (for minimum collector of 20μ with 5μ lap error)
5. N+ Buried Layer: $R_{CS} \leq 15$ ohms/square

---

1. Wafer Stock: 2 ohm-cm, n-type < 100 >, 20 ± 0.5 mils, 1-3/8" diameter.

2. Parallel Lap & Polish: Dallons machine lap to 12 mils; jig lap of three wafers together, one side 8 to 9 mils, polish one micron grit, finish with 1/4-micron to specular appearance; mount on jig polish side down and lap parallel. Measure five places on wafer and record average.

3. Clean: Three separate concentrated H_2SO_4 + 5% HNO_3 baths at 150°C, and 1 bath of concentrated HNO_3 at 55°C; 5 minutes in each bath. DI rinse; methanol; blow dry.

4. Oxidation: 16,000 Å thermal. Overnight 1020°C, 90° on bubbler.

5. PR Collector Isolation I: (Mask #428-1N) Shipley Az 111, oxide etch approximately 8 minutes.

   PR Collector Isolation II: Same as Isolation I.

6. Clean: Same as Step 3.

7. Collector Isolation Etch: Wax mount on Teflon disk, etch for 30 ± 5 microns across wafer using 2:15:5 etch. Demount, degrease.

   Oxide Etch: HF until nonwettable.

8. N+ Collector Buried Layer Diffusion: 1300°C, 15 minutes, 2 cfh N_2, Sb_2O_3. Target values: $R_{SC} \leq 15$ ohms/square; $W_c \leq 3$ microns. Discard monitor after run.

9. Oxide Etch: HF until nonwettable.

10. Thermal Oxidation: 1020°C, 16 hours, wet O_2, 80°, 10,000 Å.

11. Poly Silicon Growth: Deposit 12 mils minimum of polycrystalline silicon.

12. Backlap: Level any protrusions using #600 Carborundum; trim edge 70-100 mils; HF oxide etch 1 ± 0.1 minutes. Scrape back side; ultrasonic wash; gang mount on single crystal side; lap poly to create flat over 95% of the three wafers; remove; record thickness of each wafer. The target thickness is obtained by adding 1.5 mils to the thickness recorded above and subtracting the original thickness of the wafer recorded in Step 2. Ultrasonic wash; mount on poly side and lap to 0.8 ± 0.1 mils above the target thickness. Demount; ultrasonic clean, and polish until single crystal islands are separated.

13. Start Diffusions: Add monitor wafer; 3 ohm-cm n-type < 100 >, same ingot as substrate. Fill in diffusion times on this process sheet.

14. Clean: Same as Step 3.

15. Thermal Oxide: 5000 Å overnight (16 hours) at 900°C wet O_2, 80° on bubbler,

16. Photoresist Base: (Mask #428-2). Shipley Az 111.

17. Clean: Same as Step 3.

18. Base Deposition: NPB 1-1/4 at 5 and 7 at 12.

19. Distribution: 1140°C, 2-1/2 hours; N_2 + 4 cc/m O_2, 1 hour wet O_2, 80°C water. Read R_S and X_j. Target: R_{SB} = 150 ohms/square; X_j = 3.3 microns

20. PR Emitter: (Mask #428-3). Shipley Az 111.

21. Clean: Same as Step 3.

22. Measure: Measure BV_{CBO} test transistors.

23. Emitter Diffusions: 1140°C, _____ minutes, 150 cc/m PH_3, 50 cc/m O_2, 2.0 cfh N_2.

    Oxide Etch: Read R_S and X_j. Target: $R_S \leq 2.5$ ohms/sq., W_E = 2.5 microns, W_B = 3.6 microns. Then, 30 minutes 900° N_2.

24. Measure: Measure BV_{CEO} on test transistors.

25. Oxidation: 2 hours at 900°C, 90° on bubbler. Then ethyl silicate, 3000 Å. Convert 20 minutes, 900° N_2.

26. PR Contacts: (Mask #428-4). Shipley Az 111, remove oxide on back.

27. Clean: Same as Step 3.

28. Oxidation: Ethyl silicate, 3000 Å.

29. Oxide Conversion: 20 minutes at 900°C.

29. PR Contacts: Same as Step 26.

30. Clean: Same as Step 3.

31. Beta Adjust: 1020°C and 900°C.

Figure 3.1. Substrate Processing Sequence

1/07/69

M0A10 PROCESSING

Started: _____ Run No: _____

Ingot No: _____

Finished: _____ Wafer: _____

OPERATION	DATE	OPER-ATOR	TEMP.	TIME	R_S	X_j	W_{ox}	REMARKS	REF. NO.	INSP.
1. Wafer Stock										
2. Parallel Lap and Polish										
3. Clean										
4. Oxidation										
5. PR Col. Iso. I										
6. Clean										
7. Col. Iso. Etch										
8. N+ Col. Buried Layer Diffusion										
9. Oxide Etch										
10. Thermal Oxidation										
11. Poly Silicon Growth										
12. Backlap										
13. Start Diffusions										
14. Clean										
15. Thermal Oxide										
16. PR Base										
17. Clean										
18. Base Deposition										
19. Distribution										
20. PR Emitter										
21. Clean										
22. Measure BV_{CBO}										
23. Emitter Diffusion										
24. Measure BV_{CEO}										
25. Oxidation										
26. PR Contacts										
27. Clean										
28. Oxidation										
29. PR Contacts										
30. Clean										
31. Beta Adjust										

Figure 3.2. Substrate Processing Information

MOA10 SURFACE PROCESSING

Circuit Type: _____ **Wafer:** _____

Mask: _____ **Ingot:** _____

Lot: _____ **MJO No:** _____

	OPERATION	DATE	OPER-ATOR	REMARKS Temp., R_S, Time, etc.
1.	Contact Metal - Std. clean & oxide etch, deposit 600 Å Ti, 6000 Å Al, T_S = 100°C.			
2.	P.R. Contact Metal - KTFR, black-field mask.			
3.	Etch - Al etch, R.T. Ti etch (HF), R.T.			
4.	P.R. Removal - J100			
5.	Sinter - 450°C for 30 min. in argon			
6.	Etch - Al etch, 90°C Ti etch (HF), R.T.			
7.	Mask Metal - Degrease, deposit 5000 Å Al, T_S = R.T.			
8.	P.R. Reverse Cermet - KTFR, White-field mask			
9.	Etch - Al etch, R.T.			
10.	P.R. Removal - J100			
11.	Cermet - Std. clean, deposit 2000 ohms/square cermet, T_S=185°C			
12.	Etch - Al etch, 90°C			
13.	Top Metal - Std. clean, deposit 600 Å Ti, 12000 Å Al, T_S = 100°C			
14.	P.R. Top Metal - KTFR, black-field mask			
15.	Etch - Al etch, R.T. Ti etch (H_2SO_4), 60°C			
16.	P.R. Removal - J100			
17.	Sinter - 450°C for 20 min. in argon			

FIGURE 3.3. Surface Processing Sequence and Information

2) Dielectrically isolated integrated circuits represent the inevitable direction in which the industry will proceed in order to realize optimized circuitry.

3) This technology, combined with thin film resistors, offers good resistance to the effects of radiation.

4) The part-to-part interaction, which is a troublesome issue with high gain amplification, is minimized.

5) The collector-to-substrate breakdown voltage is high without incurring the residual effect of increased leakage currents.

6) Parasitic substrate capacitances are reduced.

7) The TRW Systems Microelectronics Center contractually pioneered the oxide isolation technique and therefore is well equipped to pursue this technology.

Disadvantages of this technology are presently the increased fabrication cost due to overall yield. Large die area, occasional defects in the isolation, and variations in collector thickness affect the yield negatively. However, counter balancing these issues with the above advantages shows dielectric isolation as a superior technique. The general processing steps are shown in Figure 3-4.

3.2 Components

3.2.1 Transistors

The NPN and lateral PNP transistors are diffused simultaneously and require no separate masking or diffusion steps. The electrical characteristic design requirements are:

NPN (low current)

Beta = 160 at +25°C and I_c = 5 mA

$BV_{CEO} \geq 45$ volts*

* Implying $BV_{CBO} \geq 120$ volts.

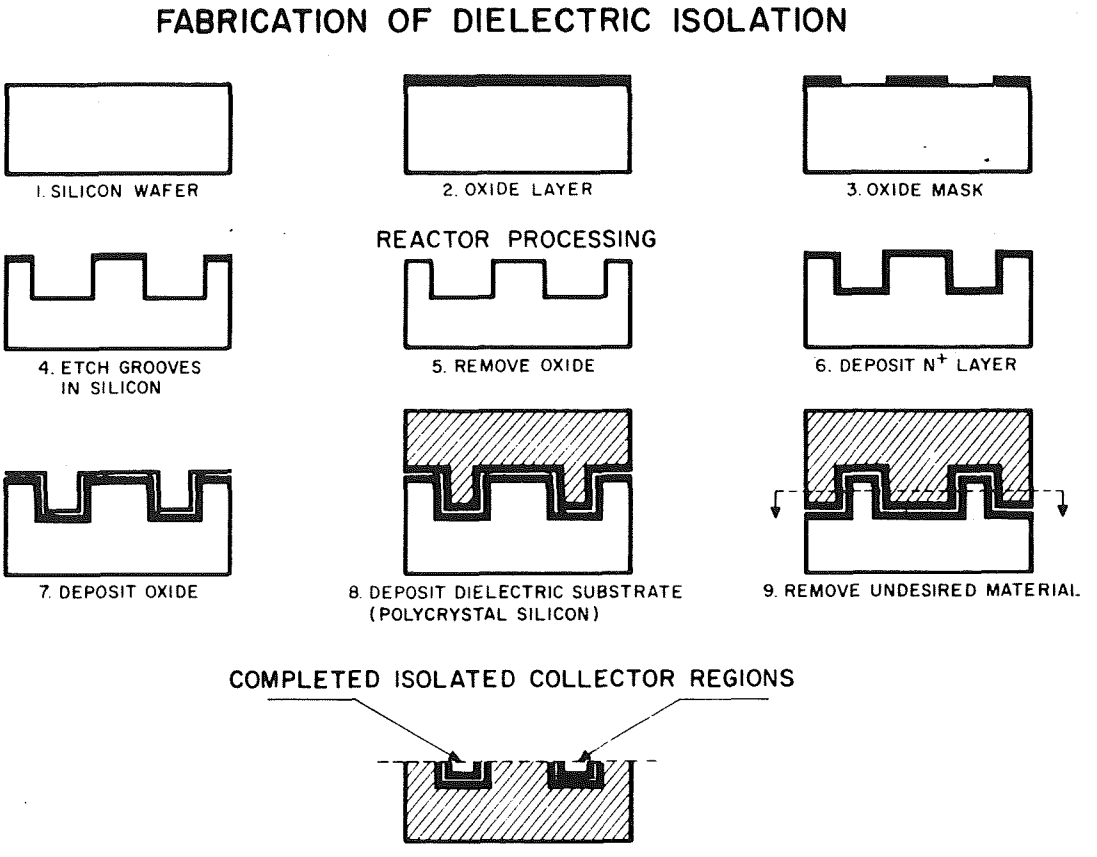

Figure 3.4. Dielectric Isolation Processing Steps

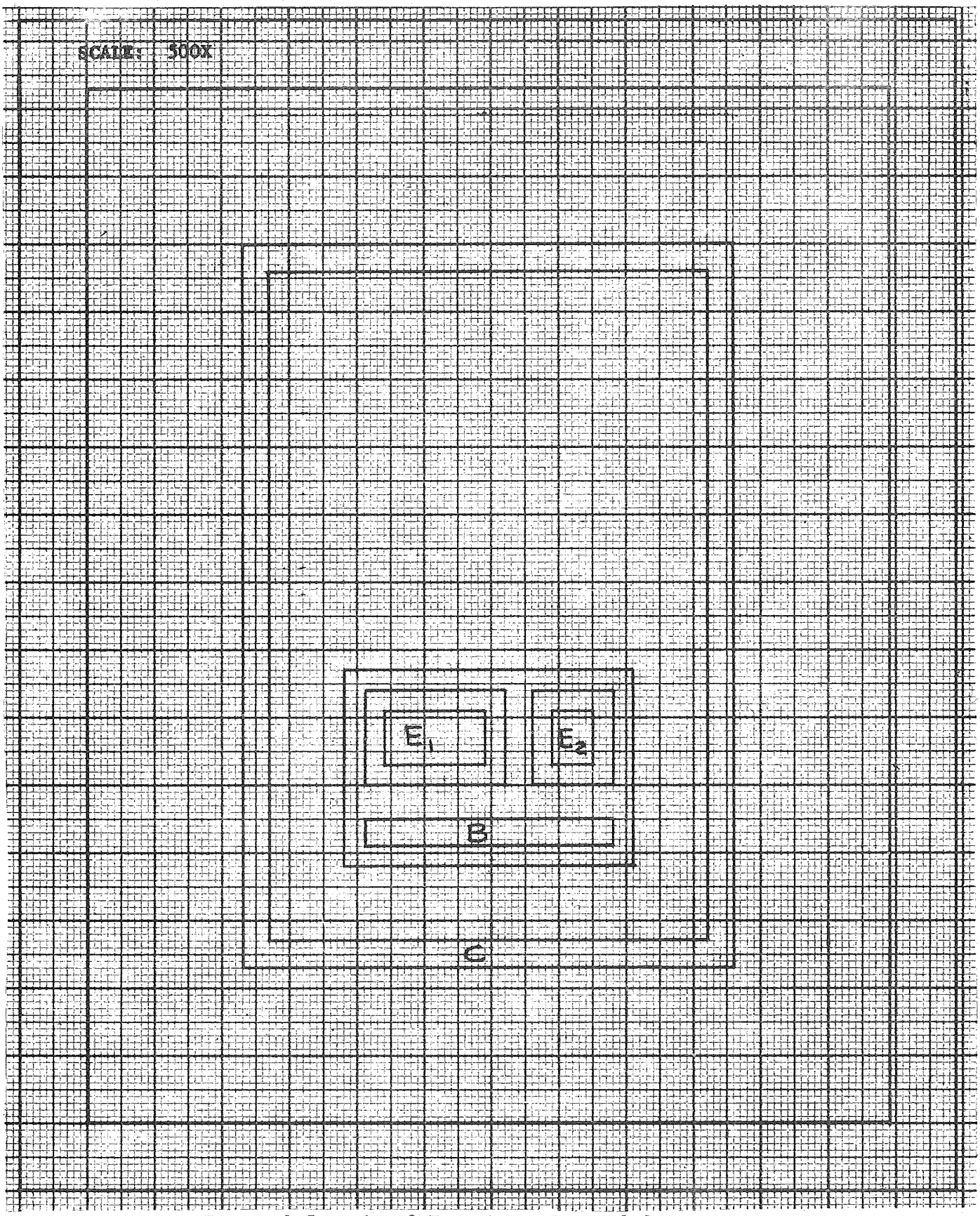

Figure 3.5. Q1, Q2 Transistor Lateral Geometry

SCALE: 500X

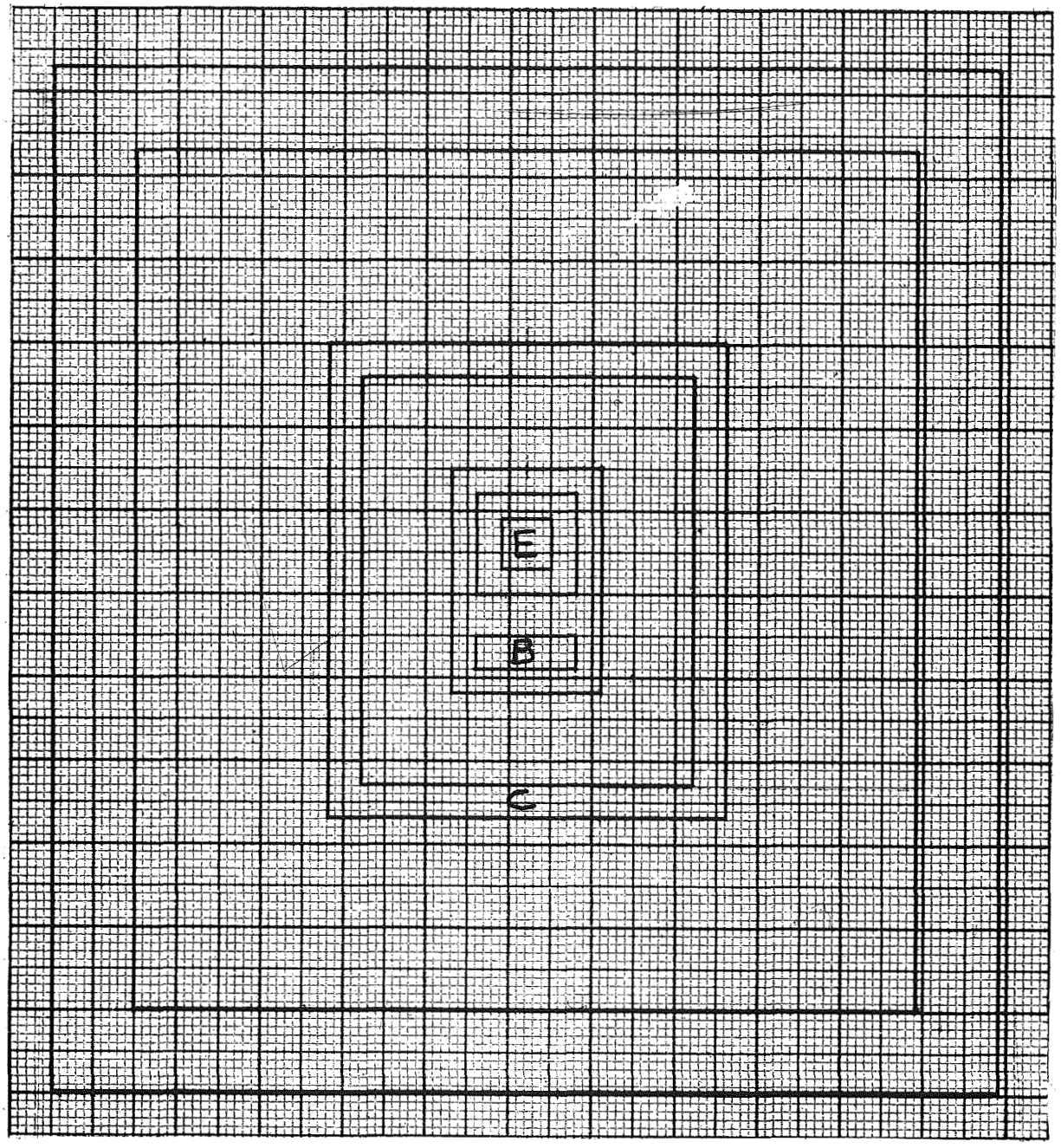

Figure 3.6. Standard NPN Transistor Lateral Geometry

SCALE: 500X

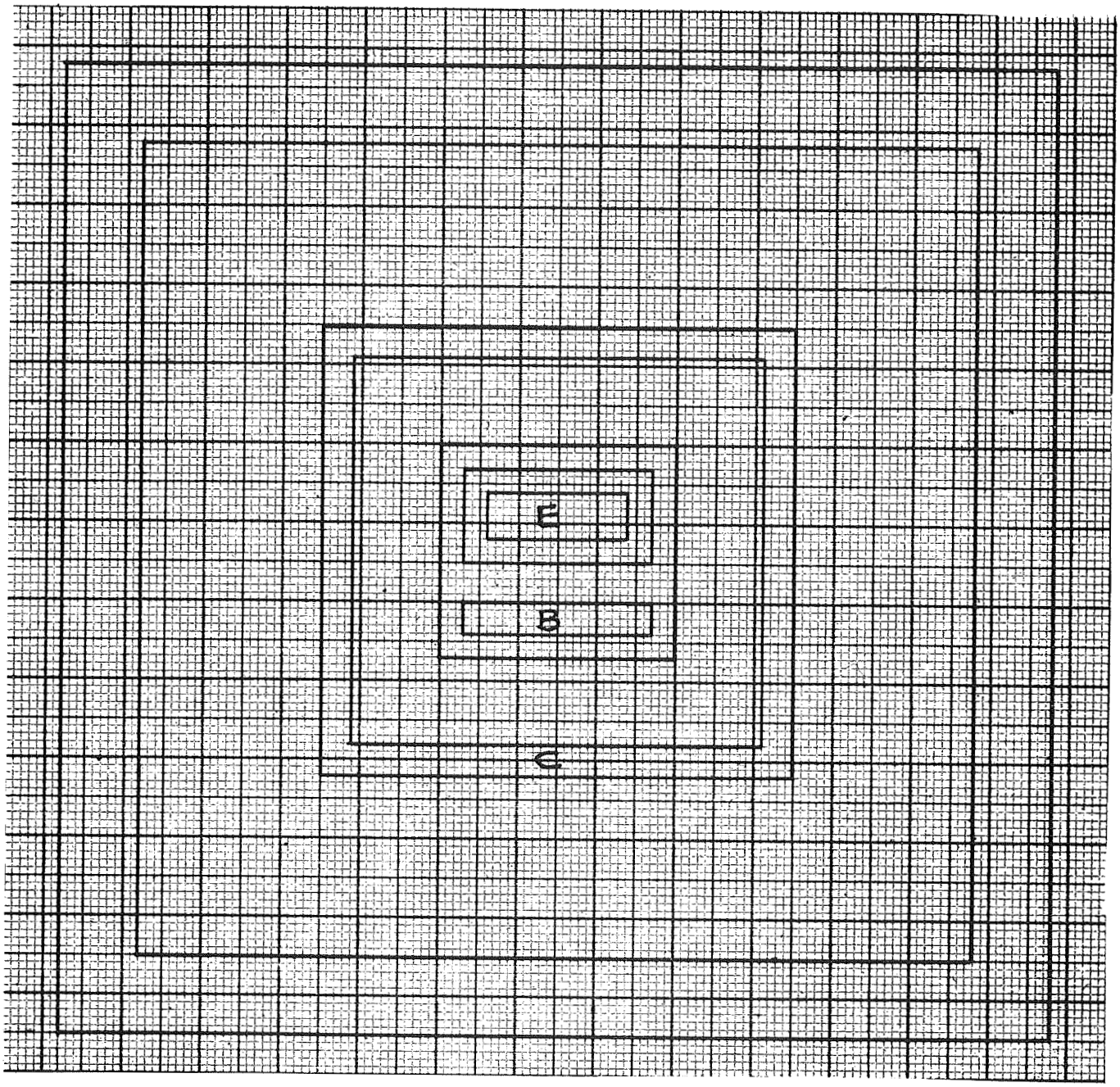

Figure 3.7. Double Emitter-Area NPN Transistor Lateral Geometry

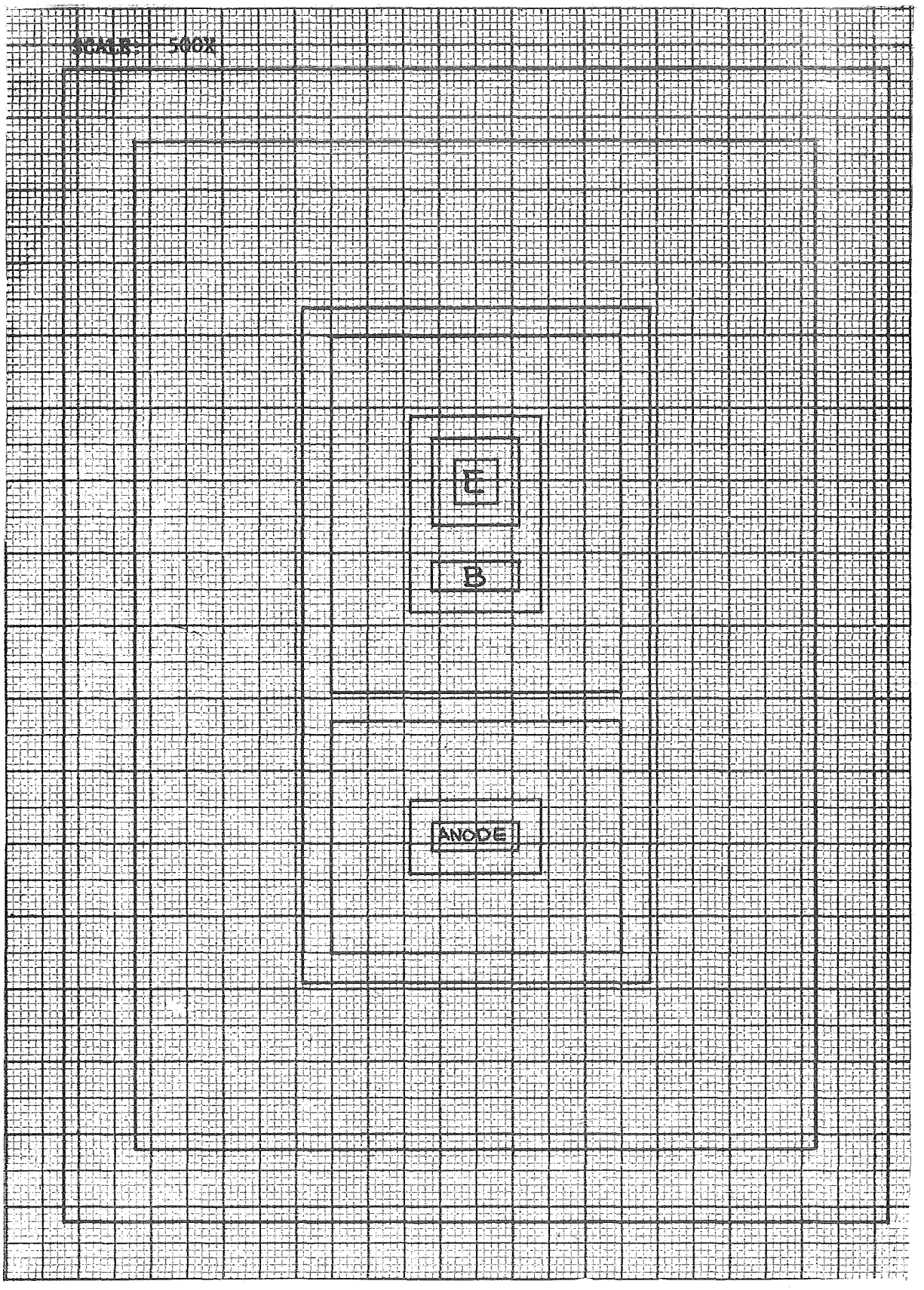

Figure 3.8. Q20, CR1 Transistor Lateral Geometry

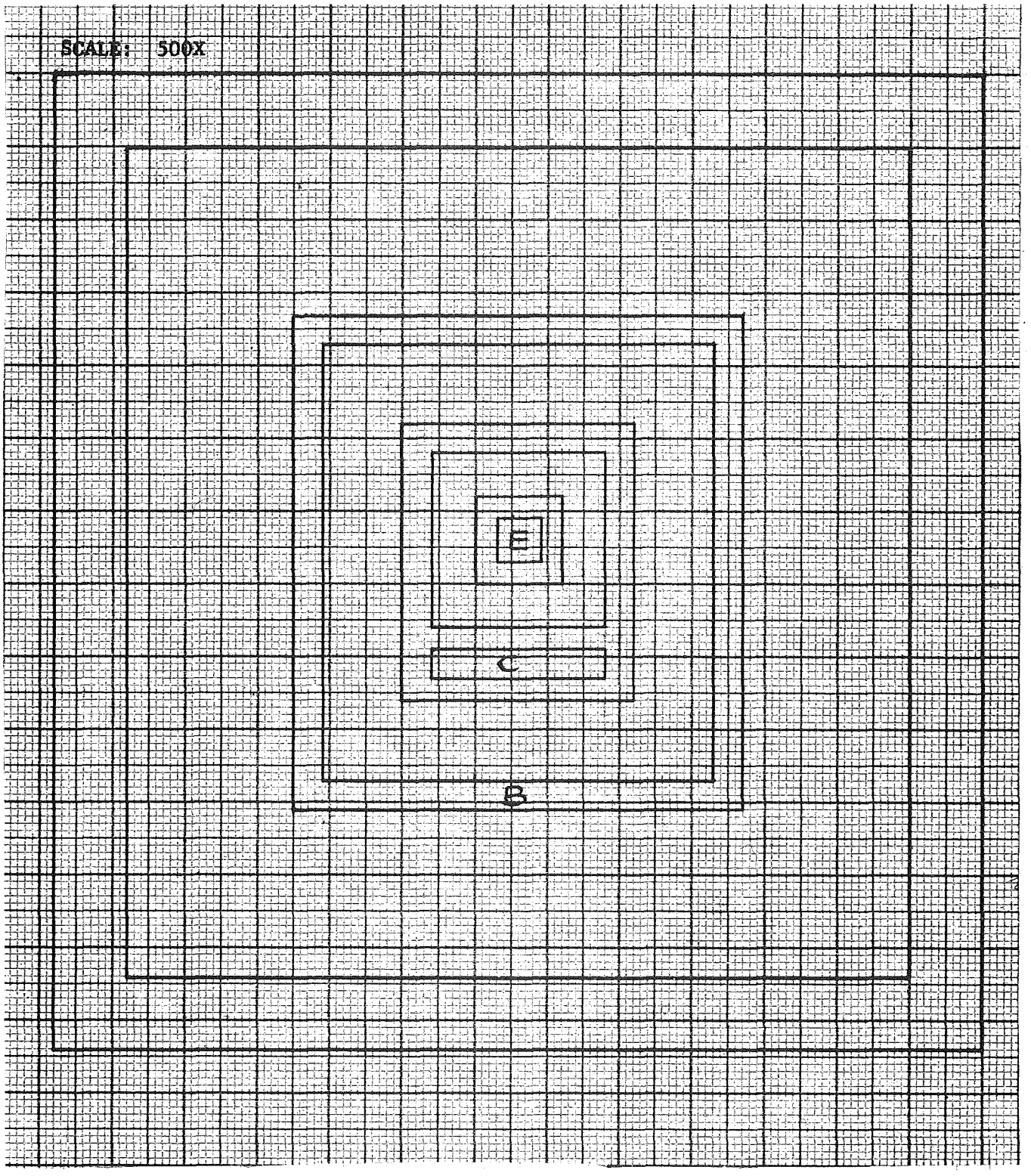

Figure 3.9. Standard PNP Transistor Lateral Geometry

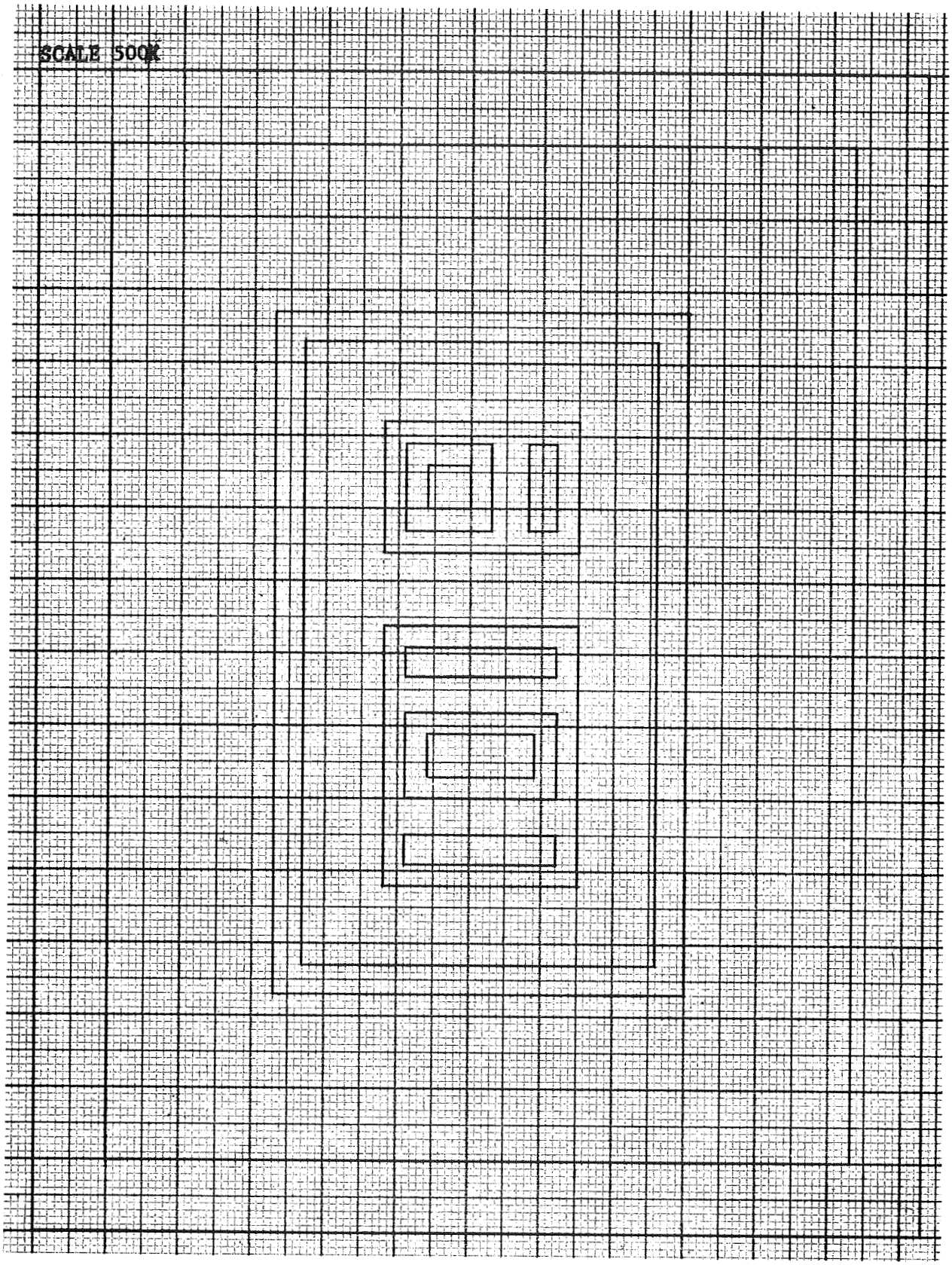

Figure 3.10. Output Emitter Follower Transistor Lateral Geometry

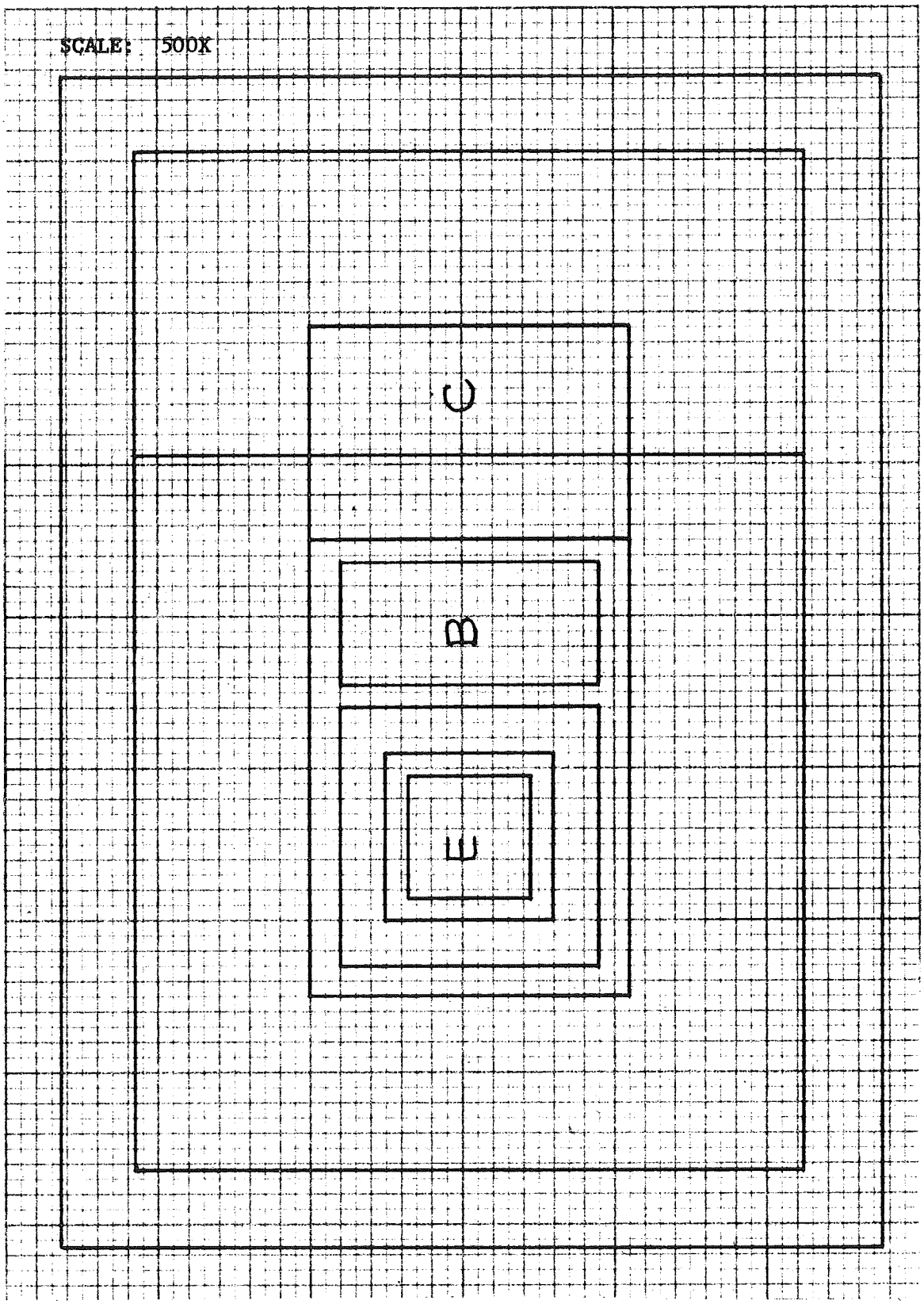

Figure 3.11. PNP Test Transistor, Transistor Lateral Geometry

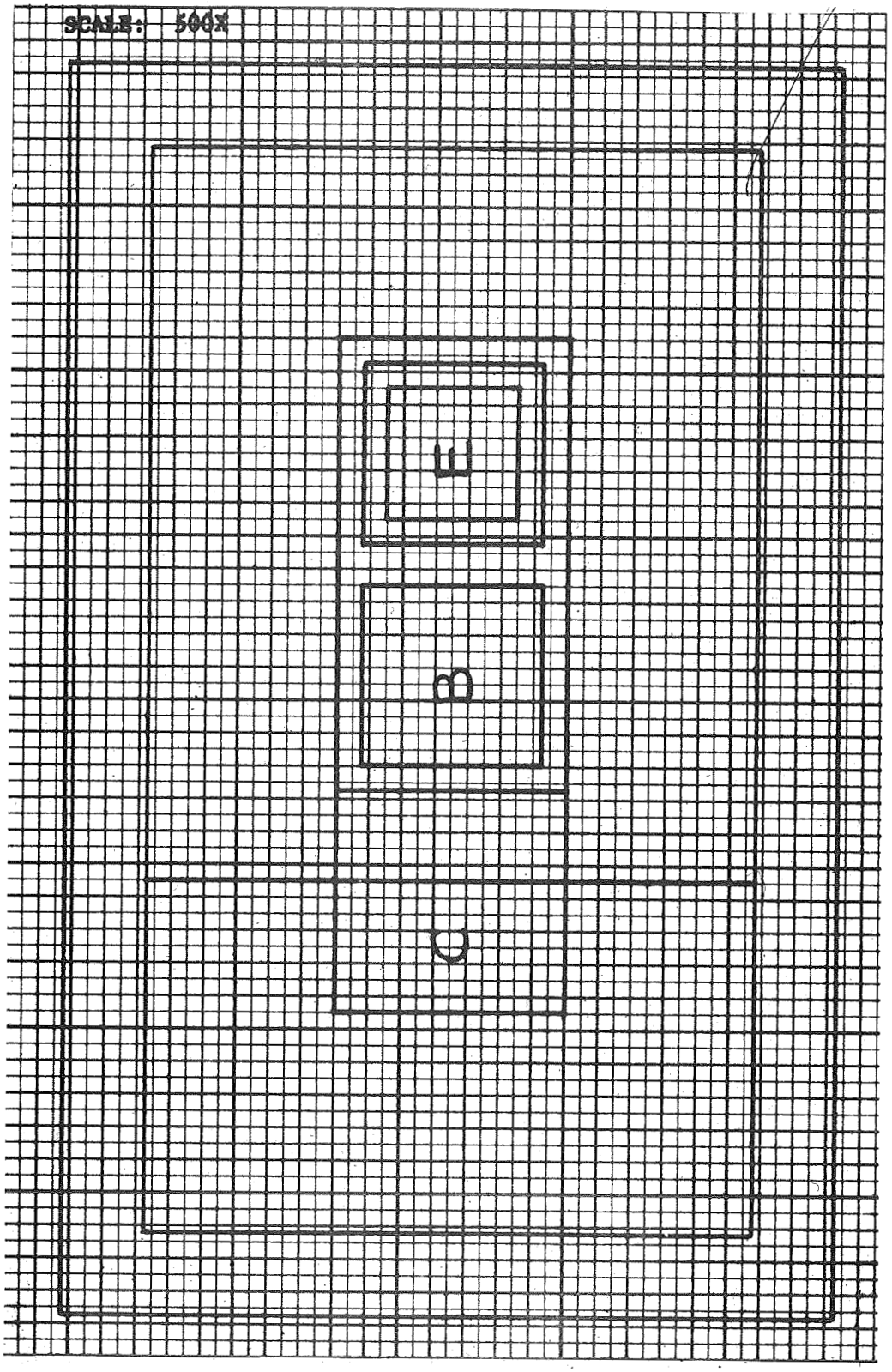

Figure 3-12. NPN Test Transistor, Transistor Lateral Geometry

NPN (high current)

Beta = 160 at +25°C and I_c = 10 mA

$BV_{CEO} \geq 45$ volts*

PNP

Beta = 1-10 at +25°C and I_c = 100 μA

$BV_{CEO} \geq 45$ volts

The base distribution target values are set at 3.3 microns depth with a surface sheet resistance of 150 ohms per square. After emitter diffusion, the base is driven in to 3.6 microns with the emitter at 2.5 microns, leaving a base width of 1.1 microns. After the contact steps (oxide removal) and beta adjust steps, the base width becomes typically 1 micron.

The lateral geometry of the devices are shown in Figures 3-5 through 3-12 to have a minimum dimensional tolerance between masks of 0.3 mil. The double emitter input transistor of Figure 3-5 illustrates the differential in the area of the two emitters required to give drift compensation. The structures of Figures 3-6 and 3-7 show the relative geometries needed for the Q_8-Q_9 current generator combination. Figure 3-8 shows the coalesced transistor-diode of Q_{20}-CR1. The lateral geometry PNP device is illustrated in Figure 3-9, while the higher current output transistor and associated Darlington current driver are shown in Figure 3-10. The test transistors of Figures 3-11 and 3-12 are used during the substrate fabrication for in-process electrical tests. Figure 3-13 shows the cross section of a typical transistor structure and thin film resistor.

---

* Implying $BV_{CBO} \geq 120$ volts.

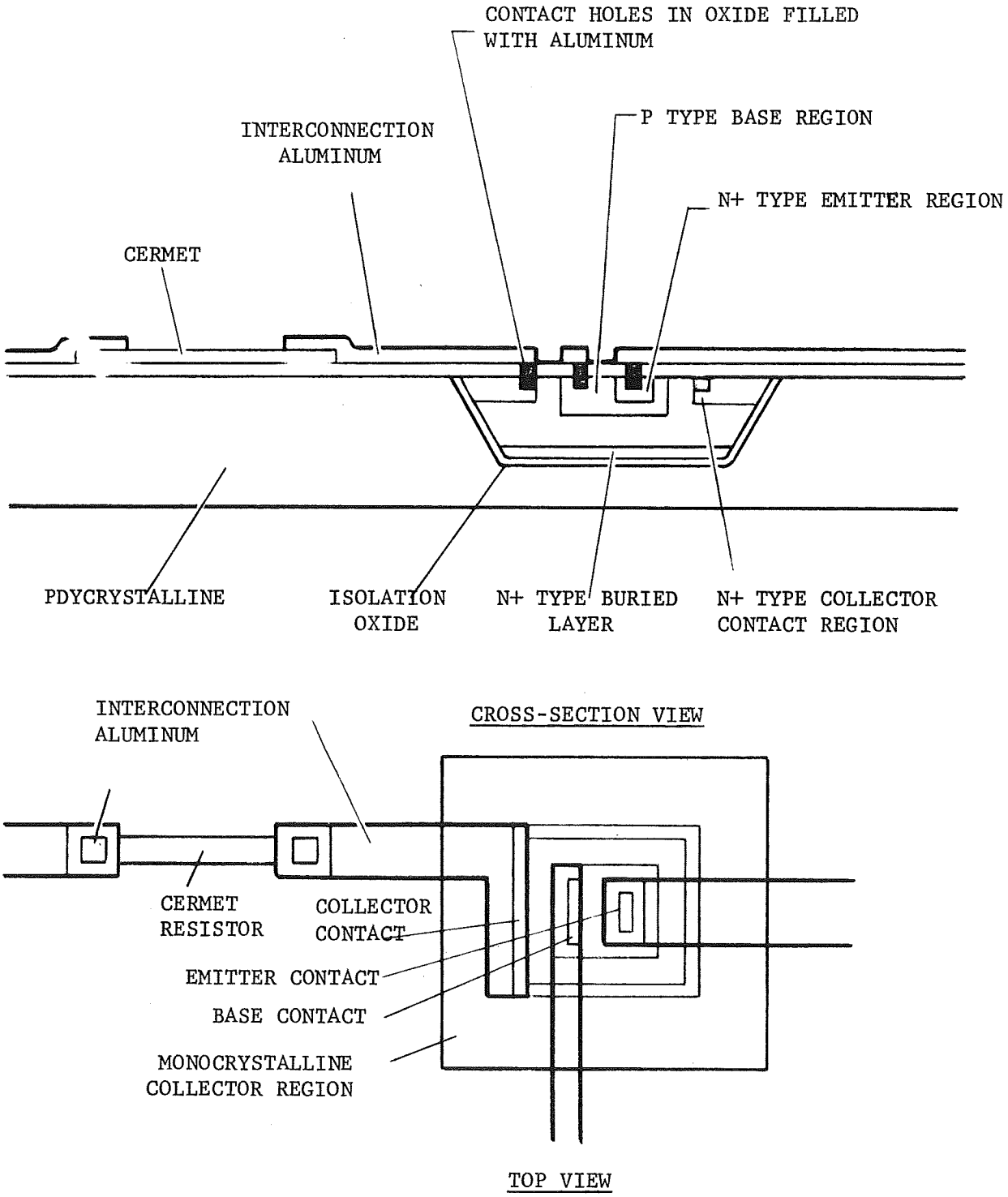

Figure 3.13. Transistor and Thin-Film Resistor Cross-Section

3.2.2 Resistors and Metallization

The resistors are formed by evaporating 150 angstroms of Cr-SiO cermet film, deposited at 2000 ohms per square. Resistor widths of 0.8 mil are typical with 0.8 mil spacing. Large incremental adjustments are made by removing cermet fuses by localized laser evaporation. Small incremental adjustments are made by localized laser annealing. (See Appendix B.)

The metal lines are typically 1.0 mil wide with 0.8 mil spaces, evaporated at 12,000 angstroms thickness.

3.3 Circuit Layout

The 165-mil by 125-mil die shown in Figure 3-14 is to be divided into two groups of components. The larger input section includes all differential and associated common-mode components, from the input terminals through R_8 and R_9 (see Figure 2-1). Likewise, the smaller, output section includes all the components from Q_{5C} and Q_{5D} through to the output. The division is a "safety feature" which allows the sections to be separately diced in the event the processing yield is low, since 97 devices is recognized as a relatively complex circuit for a high-precision analog function. In the event of a reasonably high yield, single-die monolithic amplifiers would be selected for packaging. In the event of a low yield, a two-die amplifier (composed of an input section and an output section) would be packaged.

The input and output sections are electrically connected with only four wires, two signal lines, and two power lines. When a high yield is established, these interconnections can be made via the aluminum

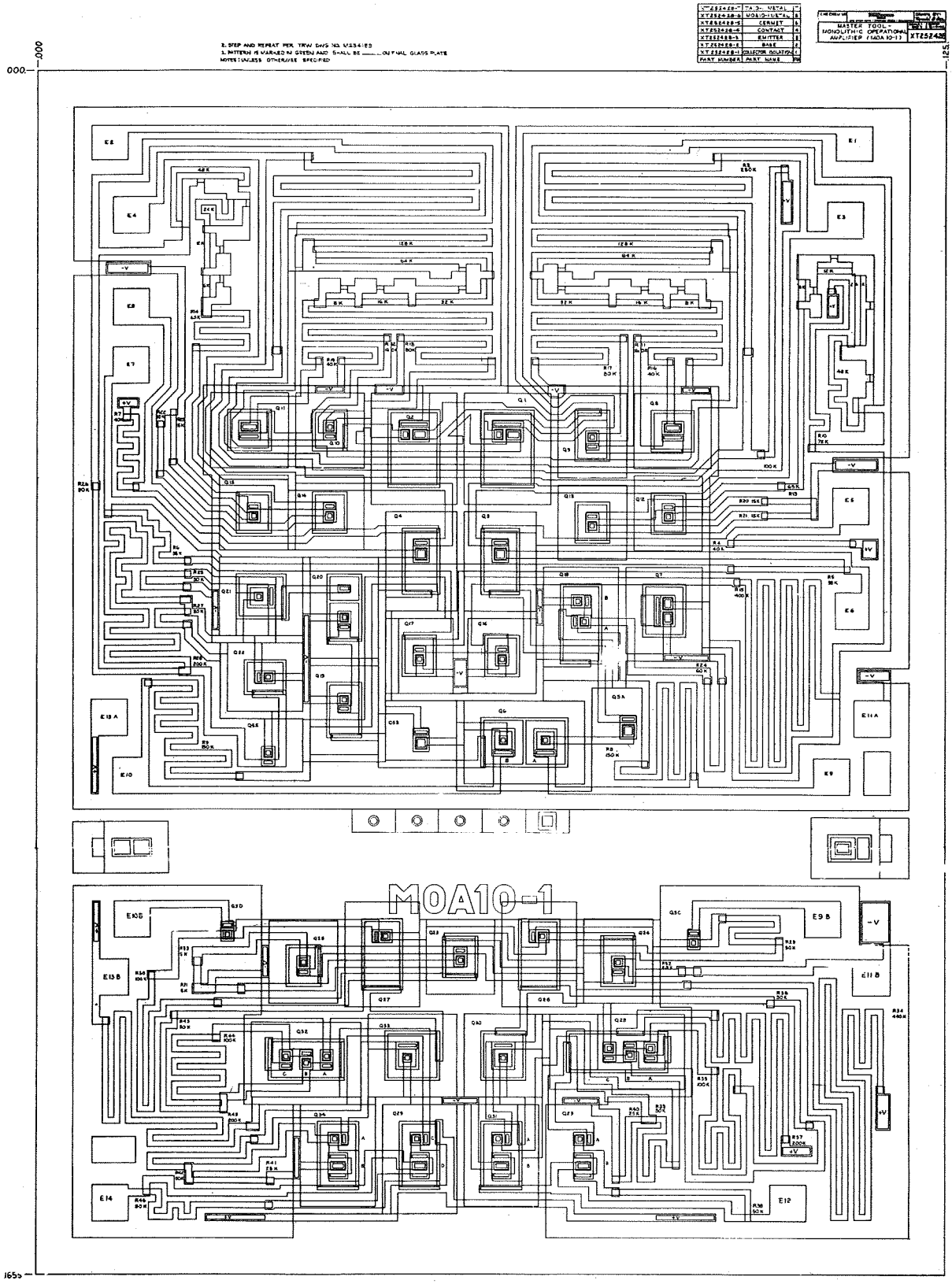

Figure 3.14. MOA-10 Integrated Circuit Layout

metallization by making a simple change in the metal mask.

Note a few features of this circuit layout:

1) The positive supply potential is distributed via the monocrystalline silicon which lies under the resistor pattern.

2) The negative supply potential is distributed via the polycrystalline silicon which lies between the monocrystalline tubs.

3) The output transistors, Q_{29B}, Q_{29D}, Q_{31B}, and Q_{34B} are arranged so that the thermal differentials observed by the input transistor pair are minimized as the output is driven from one extreme to the opposite. This is done to reduce the effect of thermal feedback.

4) Note the fuse links of R_{11}, R_{12}, R_{13}, and R_{14}.

5) The test transistors and line-up pattern are placed in the cut-away strip between the input and output sections.

6) The bonding pads lie on the periphery of the die.

3.4 Packaging and Wiring

Figure 3-15 shows the cutaway of the transparent covered package. The Corning 7059 glass-topped package allows laser trimming after the package has been sealed and while the circuit is energized. Therefore, the electrical parameter changes which occur during sealing are unimportant since final adjustments occur later. Also, a circuit characteristic, such as output offset, can be measured directly during the adjustment cycle. In addition, the transparent cover allows the circuit to be visually inspected after all processing steps have been completed.

The cover is processed and sealed to the package by the following procedure:

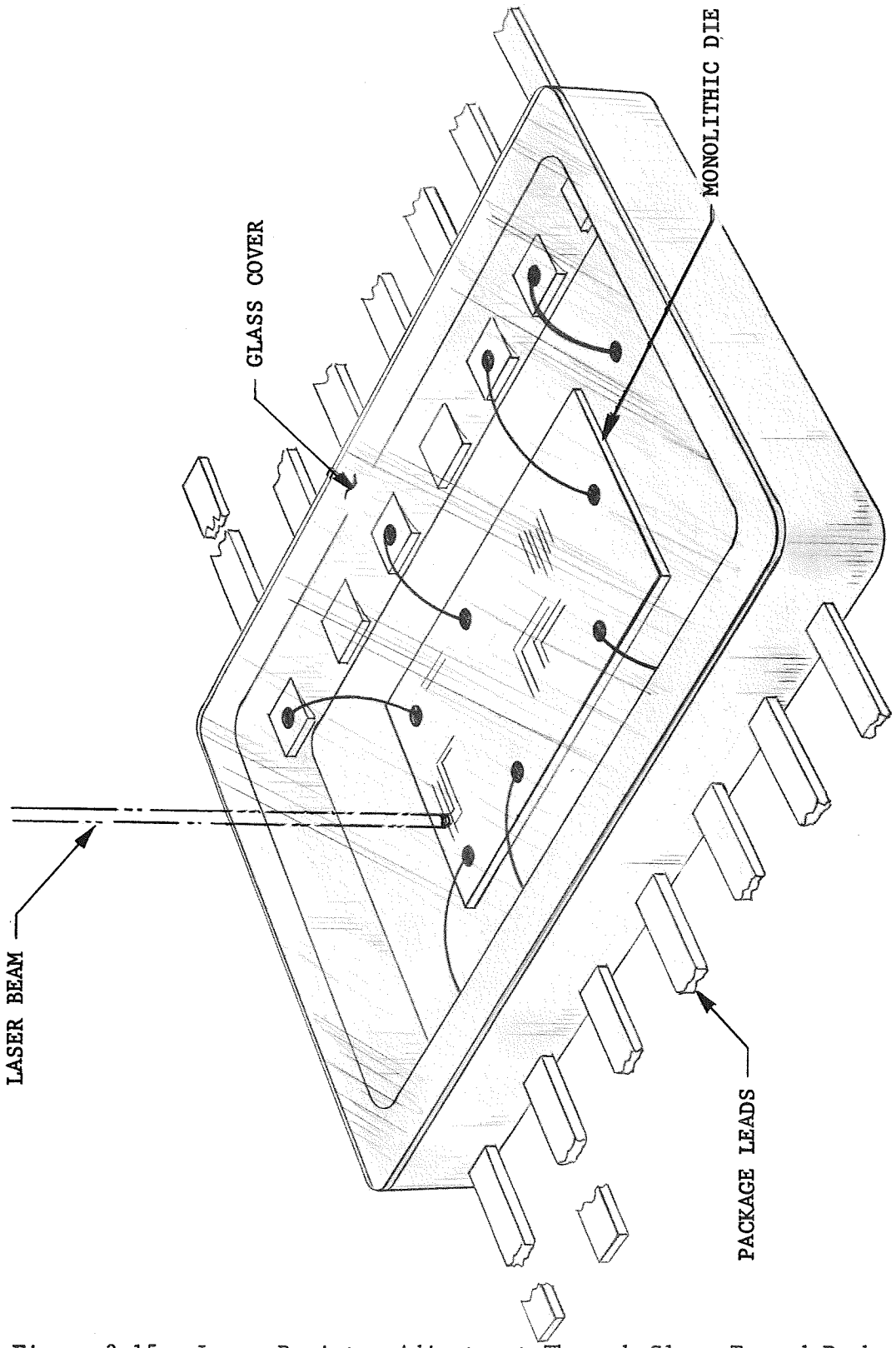

Figure 3.15. Laser Resistor Adjustment Through Glass Topped Package

1) The glass is vapor degreased in methyl alcohol.

2) Approximately 600 angstroms of aluminum is evaporated.

3) Approximately 10,000 angstroms of gold is evaporated.

4) The window pattern is photoresisted and etched. The photoresist is removed.

5) 0.1 mil of gold is electroplated on the glass.

6) The array is sawed into individual tops.

7) The top is eutectic soldered to a 1/4-inch by 3/8-inch, fourteen-lead metal bottom package (See Figure 3-16), using a gold-tin preform. The sealing is performed at 320°C in an N_2 environment.

Hermeticity measurements, using the helium leak test, show typical seals of 5×10^{-8} cm of Hg.

Figures 3-16 and 3-17 show the package dimensions and the wiring diagram, respectively.

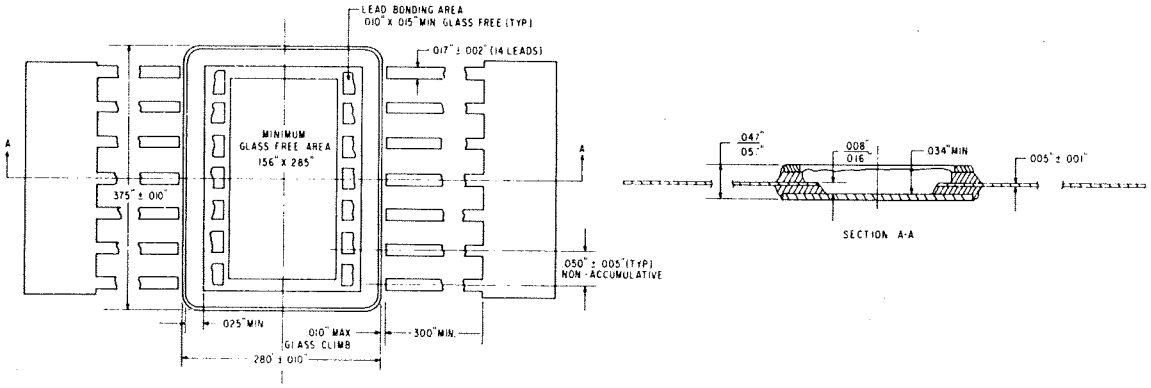

Figure 3.16. Flat Package Dimensions

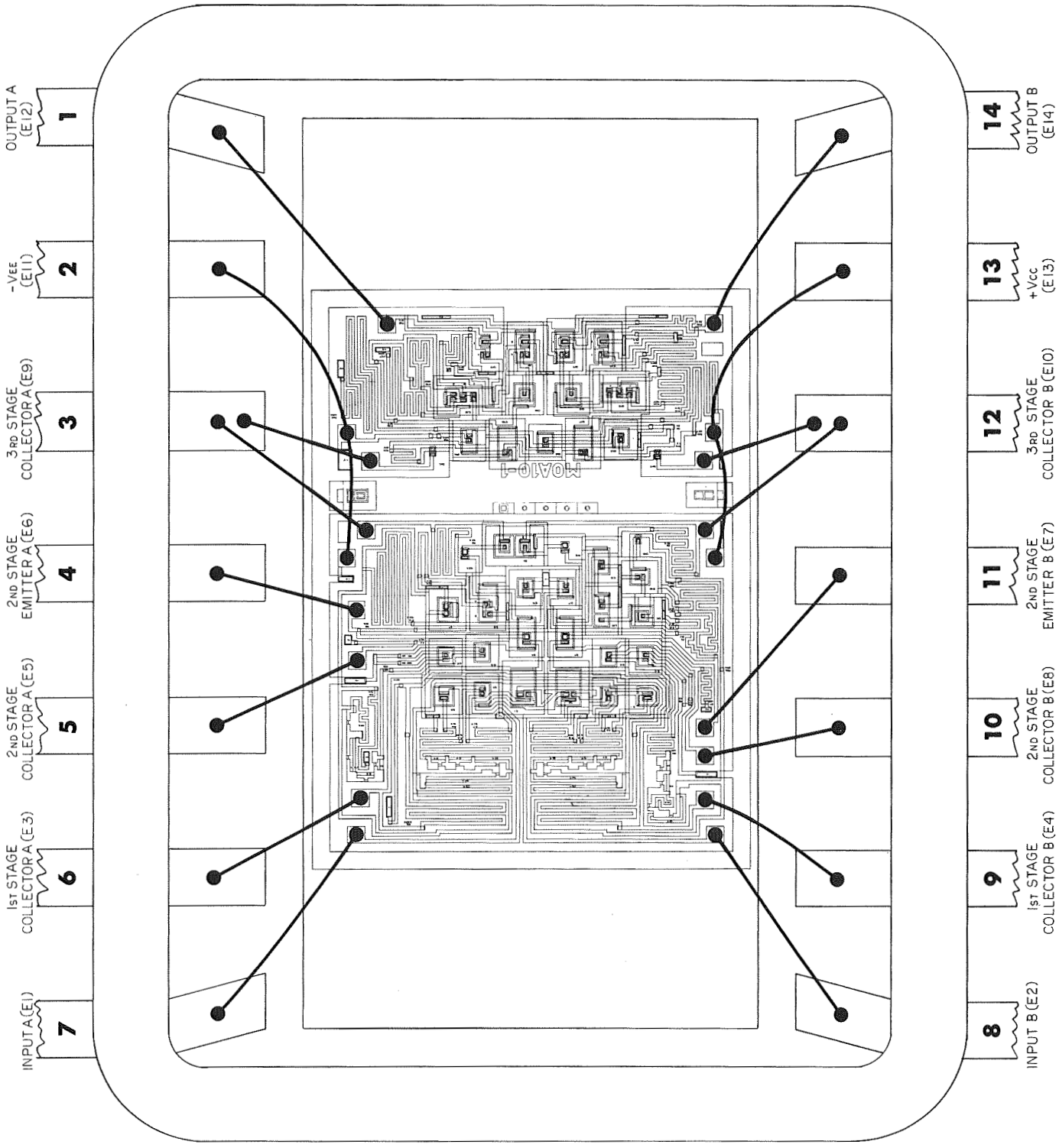

Figure 3.17. MOA-10 Package Wiring Diagram

4.0 TESTING AND EVALUATION

4.1 The wafer test set is shown schematically in Figure 4.1. The input and output sections are tested separately, according to the following steps:

Switch Position	Function Description
1	The input section is driven with an ac signal so that the output limits. The input-output transfer function characteristics are monitored on the x and y coordinates of an oscilloscope. Output voltage swing and gain are measured from the oscilloscope.
2	The input section input voltage is set to zero. The outputs are tied together and the common-mode output voltage read directly with a digital meter.
3	A dc voltage is applied to the input section so that the output differential voltage is driven to zero. The dc input voltage is read as the equivalent input voltage offset. Then the power supply current is measured.
4	The output stage power supply current is measured.
5	The output section is driven with an ac signal so that the output limits. The input-output transfer function characteristics are monitored on an oscilloscope. Output voltage swing, with a 5 K load and gain are measured from the oscilloscope.

Figure 4.2 shows the form which is used to record the above measurements. If one section is found acceptable with the other not acceptable, the die is cut in two, so that the functional section can be used in a two die amplifier configuration. If both input and output sections are acceptable, the die is further processed as a monolithic amplifier.

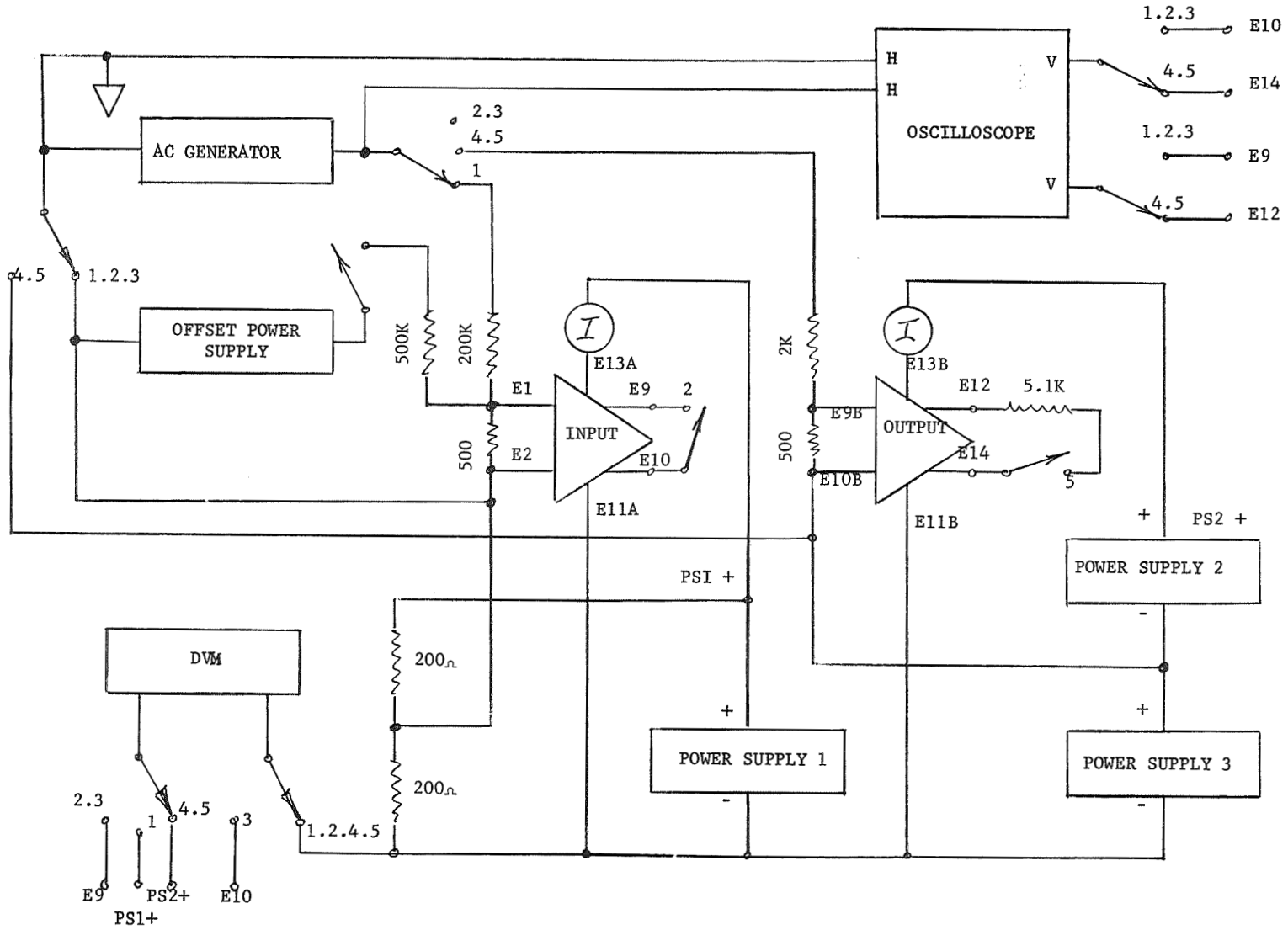

Figure 4.1. MOA-10 Wafer Test Circuit

RUN _____ WAFER _____ MOA-10 WAFER TEST INFORMATION DATE _____ OPERATOR _____

	INPUT STAGE						OUTPUT STAGE			
Die. Pos.	V_S	$V_{o\text{-}swing}$	A_{vi}	$V_{o\text{-}cm}$	$\equiv V_{io}$	I_S	V_S	I_S	$V_{o\text{-}swing}$	A_{vo}

Figure 4.2

MOA MODULE ASSEMBLY 5-8-69

	Run	Wafer	Position	Date	ID
1. Die Selection:					
Complete					
Input					
Output					
2. Record Wafer Test Data					
3. Module Identification Mark					
4. Module Cleanup and Inspection					
5. Mount Die					
6. Bond					
7. Dress Leads					
8. Visually Inspect					
9. Functional Test No. 1					
10. Cleanup and Inspection					
11. Bake out at 150°C for 15 Minutes					
12. Seal with Transparent Cover					
13. Measure Hermeticity					
14. Functional Test No. 2					
15. Adjust Drift-Offset with Laser					
16. Long Term Bake Out					
17. Final Adjustment with Laser					
18. Final Test No. 3					

	Wafer	Test #1	Test #2	Test #3
A_{VO}				
V_O(max) at R_L = 5K				
V_O(min) at R_L = 5K				
I_S at V_S = 45 volts				
$\equiv V_{io}$				
V_O-cm				
R_O				
CMR				
f_{co}				
ϕ_s				
V_{oo} at +125°C				
at + 75°C				
at + 25°C				
at - 25°C				
at - 55°C				

Figure 4.3

4.2 Module Test Procedure

The MOA-10 modules are assembled according to the sequence shown in Figure 4.3. Each amplifier has traceability back to ingot and wafer information, with the processing data recorded on the forms shown in Figures 3.2 and 3.3.

The electrical testing of the monolithic amplifiers was performed according to the following procedure:

4.2.1 Open Loop Gain - Output Voltage Swing - Power Consumption

The test configuration shown in Figure 4.4 is used to measure these three parameters. The power consumption is measured by monitoring the current in the positive supply line, with the output load resistor, R_L = 5 K ohms, not connected.

The open loop gain and output voltage swing are measured with the output load resistor, R_L = 5 K ohms, connected. Figure 4-5 represents a typical oscilloscope pattern on which the gain and voltage swing are measured. The gain is measured as the slope times a proportionality constant, K = 10^5, determined by the external attenuators shown in Figure 4.4. The frequency of the signal source is chosen at 10 Hz to be sufficiently below the lowest natural pole of the monolithic amplifier. The gain measurement, therefore, represents the dc gain value.

The specified values are:

$$A_{VO} \geq 10^6$$

$$\overline{\Delta V_O} \geq 60 \text{ volts at } I_L = 6 \text{ mA}$$

$$P_D \leq 50 \text{ mW quiescent}$$

4.2.2 Drift

The specified output offset over the temperature range -55°C to +125°C is:

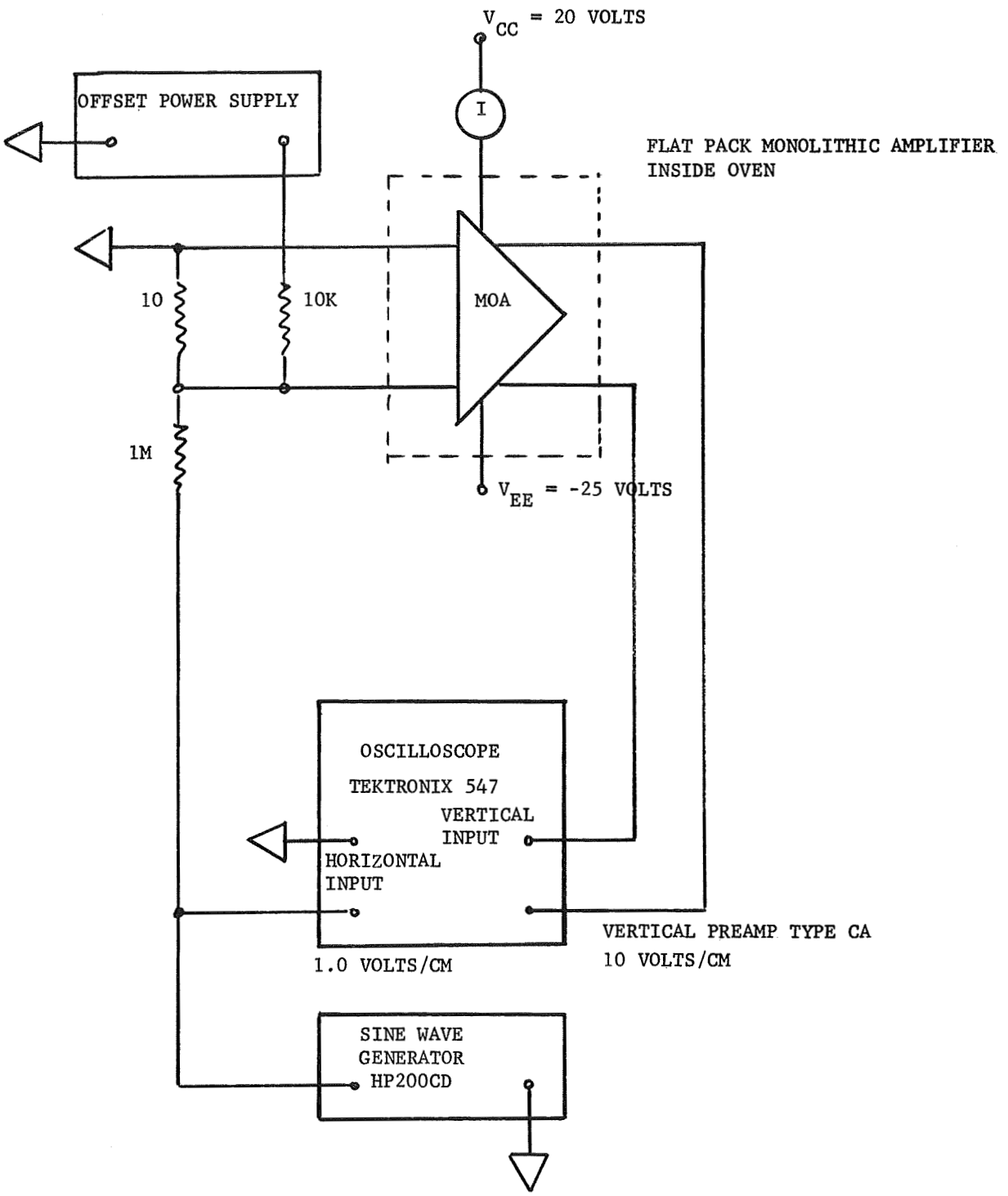

Figure 4.4. Test Configuration for Open Loop Gain, Output Voltage Swing, and Power Consumption

Figure 4.4. Test Configuration for Open Loop Gain, Output Voltage Swing, and Power Consumption.

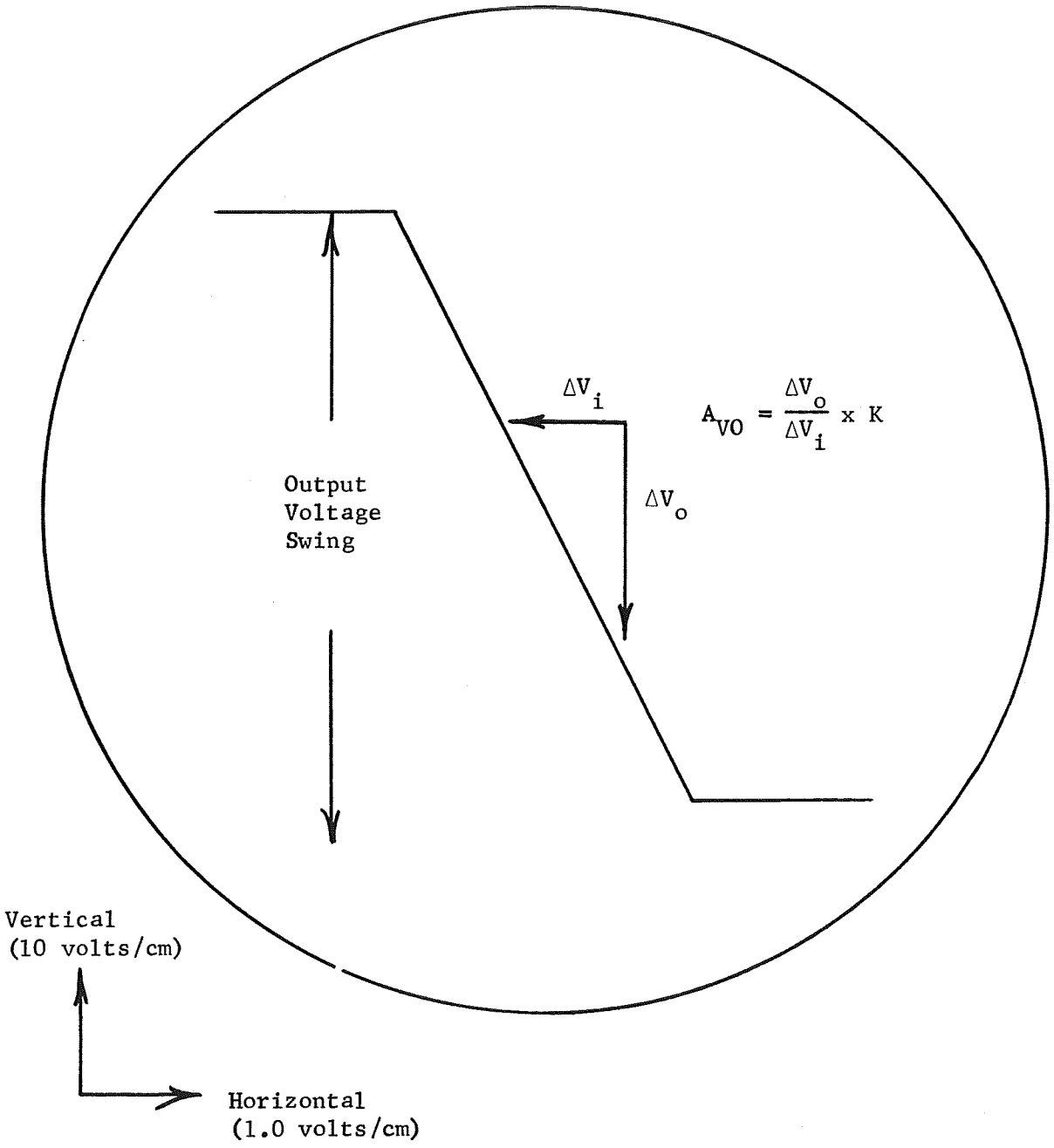

Figure 4.5. Typical Oscilloscope Pattern for Figure 1 Test Configuration

$V_0 \leq 15$ mW at closed loop gain of 10, as shown in Figure 4.6. The resistors are 1% values, symmetrically matched to 0.01% with $\pm$ ppm/°C temperature coefficient. The resistors are outside the oven, and therefore experience only room temperature ambient.

The amplifier output is monitored with a digital voltmeter while the input of the closed loop configuration is shorted and the amplifier is stabilized at the following temperatures:

+125°C

+ 75°C

+ 25°C

- 15°C

- 55°C

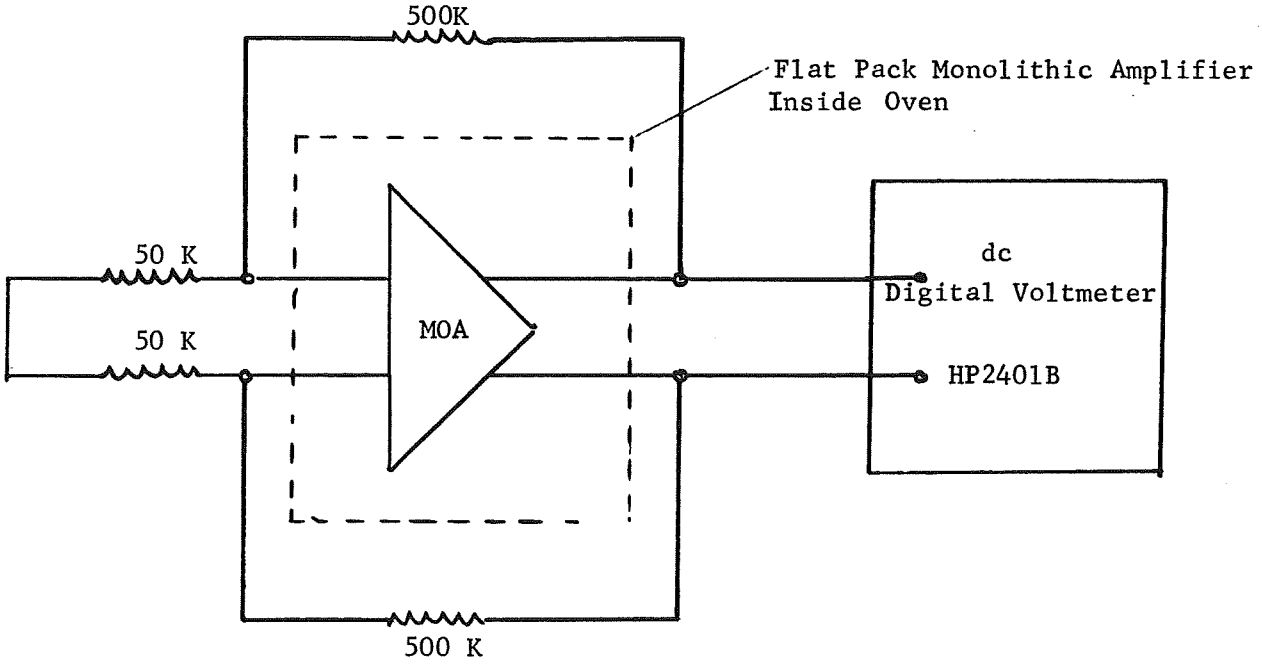

Figure 4.6. Test Configuration for Temperature Drift

4.2.3 Output Resistance

The output resistance is measured by applying a dc 1-volt differential input signal to the closed loop configuration shown in Figure 4.7. The output dc voltage is measured with and without a 5 K ohm differential load. The output voltage variation must be less than 200 milliwatts to insure that the output resistance specification is met,

$R_0 \leq 100$ ohms.

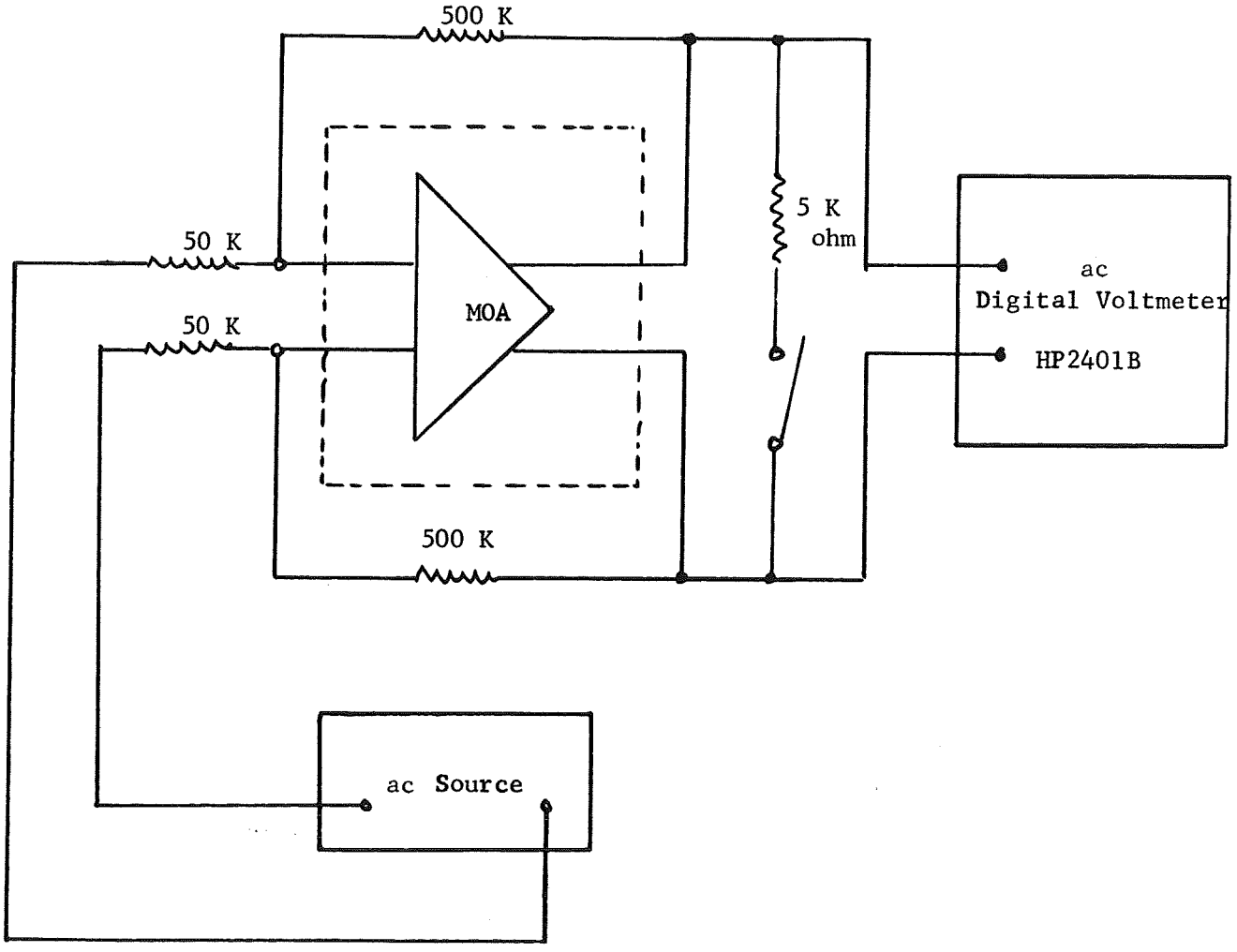

Figure 4.7. Test Configuration for Output Resistance

4.2.4 Common-Mode Rejection

The common-mode rejection is measured in the test configuration of Figure 4.8. The ac signal source is set at ±1 volt, peak-to-peak amplitude at 10 Hz. Since the specification is

$$CMR \geq 60 \text{ dB},$$

the common-mode gain must be less than -40 dB. Therefore, the meter must read less than 20 millivolts peak-to-peak, or 7.1 millivolts RMS.

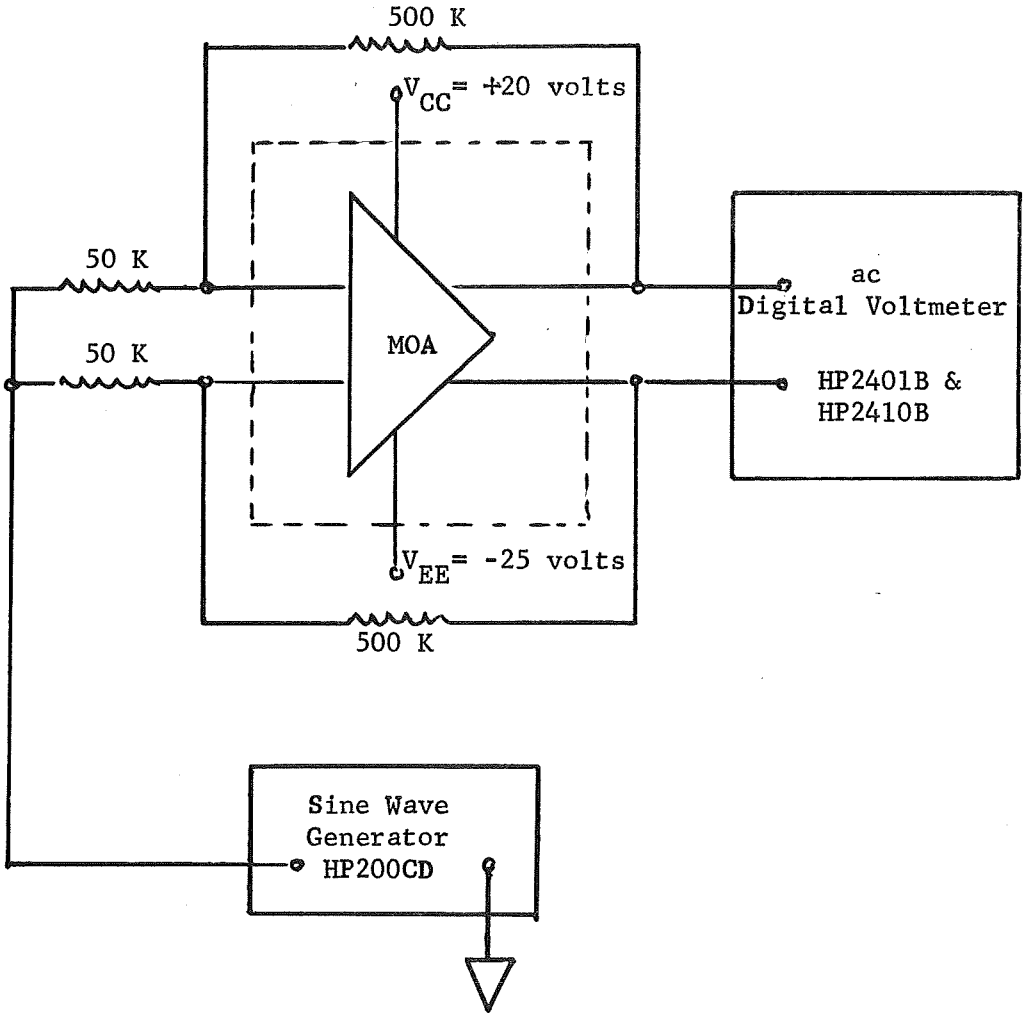

Figure 4.8. Test Configuration for Common-Mode Rejection

4.2.5 Frequency Response

The frequency response is taken by measuring the relative ac output of the closed loop amplifier at 10 Hz and 2 KHz. The 10 Hz value of gain is considered to be the same as dc. The specification states that the relative gain at 2 KHz must be 3 dB or less, below the dc value. See Figure 4.9.

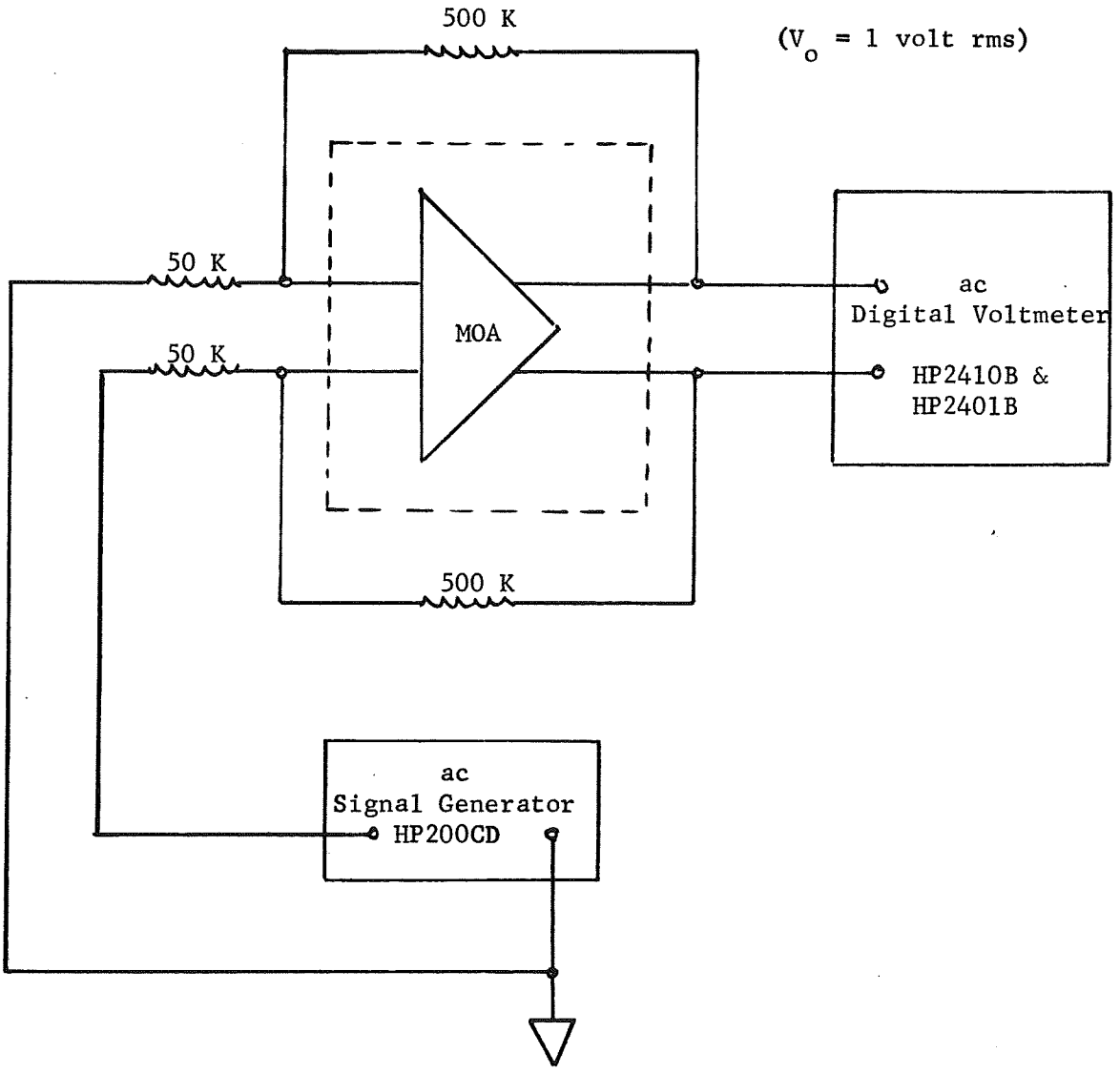

Figure 4.9. Test Configuration for Frequency Response

4.2.6 Phase Shift

The phase shift is measured by the test setup of Figure 4.10. Only one measurement, at >5Hz, is taken to insure meeting the specification 1.5° maximum phase shift.

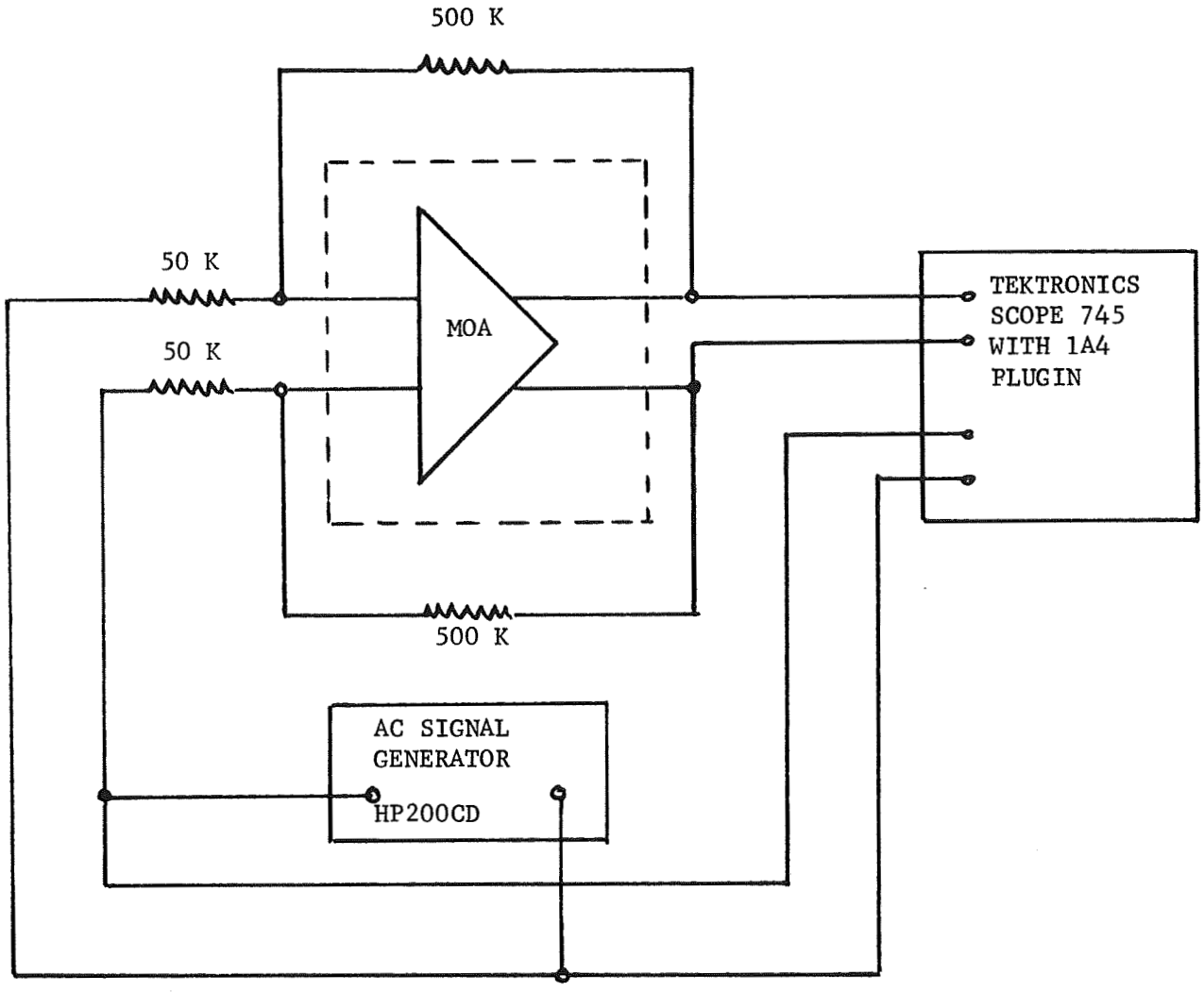

Figure 4.10. Test Configuration for Phase Shift

4.3 Test Results

Figures 4.11a and 4.11b show the test data and graphed temperature drift information, respectively for Amplifier SN 41. The other fourteen amplifiers have information shown on Figures 4.12 through 4.25. This information is summarized in Figure 4.26. Phase data was taken on only a few units to establish that 1.5° lag is typically measured at frequencies above 500 Hz, or two orders of magnitude better than spec.

4.4 Mechanical Testing

Ten functional modules were mechanically tested according to the following criteria:

Vibration:	500 g peak 200-2000-200 Hz with a 15 minute logarithmic sweep in each direction. This test will be performed in the x, y and z planes.
Shock:	100 g's for 11 milliseconds
Altitude:	Each unit should be capable of operating for an extended length of time in a perfect vacuum environment. A helium leak test and detergent bomb test will be used to test the hermetic seal of each package. The maximum leak rate is not to exceed 1×10^{-7} cc per second.

Each unit was visually examined and retested electrically and hermetically after shock and again after vibration. The resulting data is shown in Figure 4.27.

MOA-10 TEST DATA

MODULE SERIAL NO: 41

DATE: 30 JUNE 1969 RUN: 25 WAFER: 6 DIE: 30

TEMPERATURE MEASUREMENTS

	Loop Gain AV_o	Output Swing with R_L = 5K Ω	Output Offset with Zero Input
+125°C			- 7.2 mv
+ 75°C			- 0.5 mv
+ 25°C	2.5×10^6	68 VP/P	-1.5 mv
- 15°C			-10 mv
- 55°C			+ 4.5 mv

ROOM TEMPERATURE MEASUREMENTS

Power Consumption: I_S = 1.0 ma, V_S = 45 VDC, $I_S \times V_S$ = 45 mw

@ 100 Hz Output Resistance: V_o = 20. VRMS, ΔV_o < .010 VRMS, $R_o = \frac{\Delta V_o}{0.6} \times 100$ = _____

V_o^1 = _____ $R_o < \frac{.010 \times 5100}{20.} = 2.6\Omega$

Common-mode Rejection: ΔV_o(DM) = .030 VP/P, CMR = $10 \times \frac{\Delta V_o(CM)}{\Delta V_o(DM)}$ = 1,300

ΔV_i(CM) = 4 VP/P

Frequency Response: V_i = .101 VRMS V_o = 1.025 VRMS at 10 Hz, dB Attenuation = _____

V_i = .100 VRMS V_o = 1.028 VRMS at 2 KHz

Phase Shift: Ø = _____ at 5 Hz

Figure 4-11a. Amplifier 41 Test Data

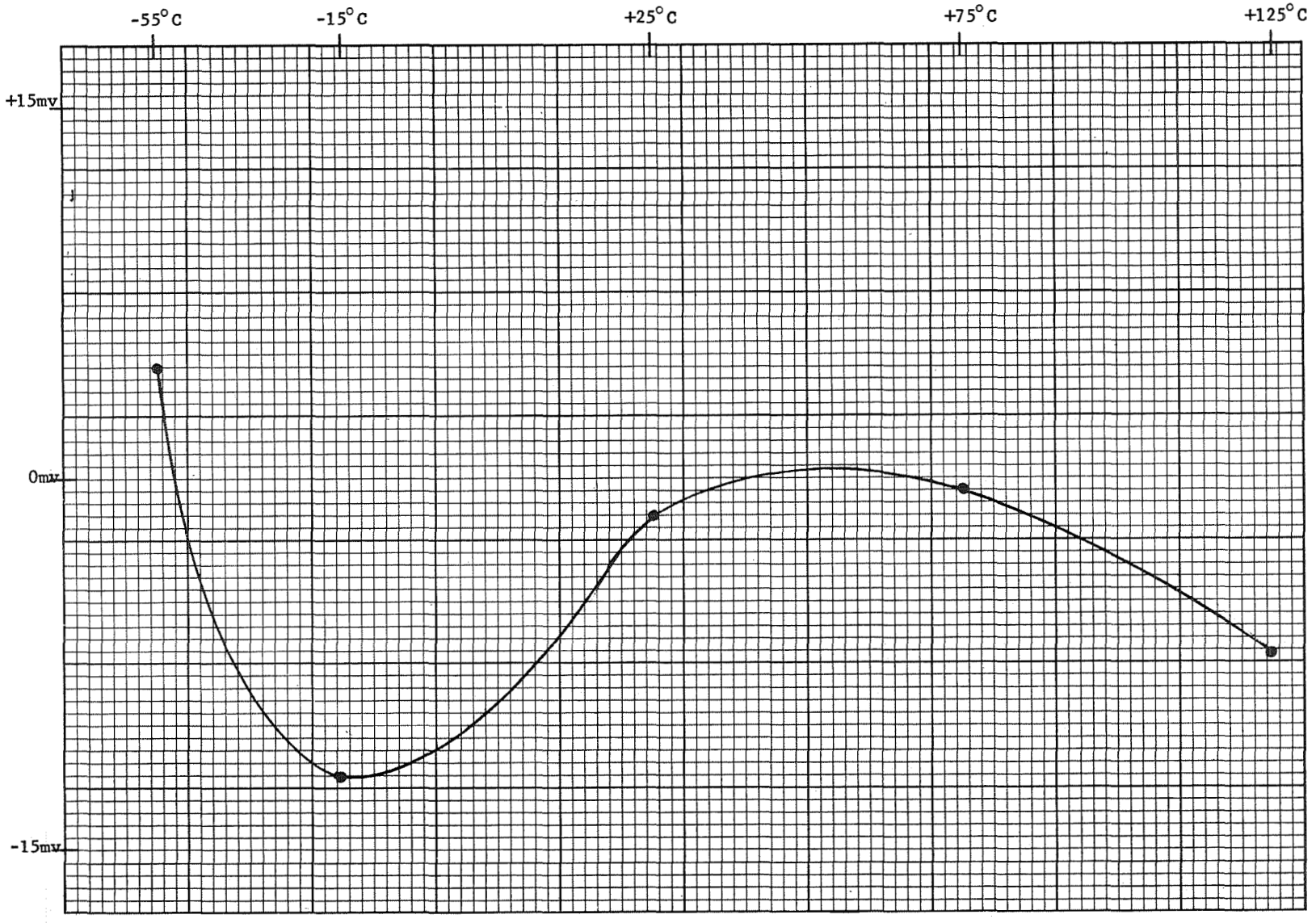

Figure 4-11b. Output Drift vs Temperature, Unit 41

MOA-10 TEST DATA

MODULE SERIAL NO: 54

DATE: 2 JULY RUN: 21 WAFER: 59 DIE: 3

TEMPERATURE MEASUREMENTS

	Loop Gain AV_o	Output Swing with R_L = 5K Ω	Output Offset with Zero Input
+125°C			-5.5 mv
+ 75°C			-6.1 mv
+ 25°C	2.8×10^6	66 VP/P	-5.0 mv
- 15°C			+1.0 mv
- 55°C			-2.8 mv

ROOM TEMPERATURE MEASUREMENTS

Power Consumption: I_S = 0.77 ma, V_S = 45 VDC, $I_S \times V_S$ = 34.8 mw

Output Resistance: V_o = 20 VRMS, ΔV_o ≤ .01 VRMS, $R_o = \frac{\Delta V_o}{0.6} \times 100$ = _____

V_o^1 = _____ $R_o \leq \frac{.01 \times 100}{20} = 2.6\ \Omega$

Common-mode Rejection: ΔV_o(DM) ≤ .004 VP/P, CMR ≥ $10 \times \frac{\Delta V_i(CM)}{\Delta V_o(DM)}$ = 10,000

ΔV_i(CM) = 4 VP/P

Frequency Response: V_i = .100 VRMS V_o = 1.013 VRMS at 10 Hz, dB Attenuation = _____

V_i = .100 VRMS V_o = 1.033 VRMS at 2 KHz

Phase Shift: Ø = _____ at 5 Hz

Figure 4-12a. Amplifier 54 Test Data

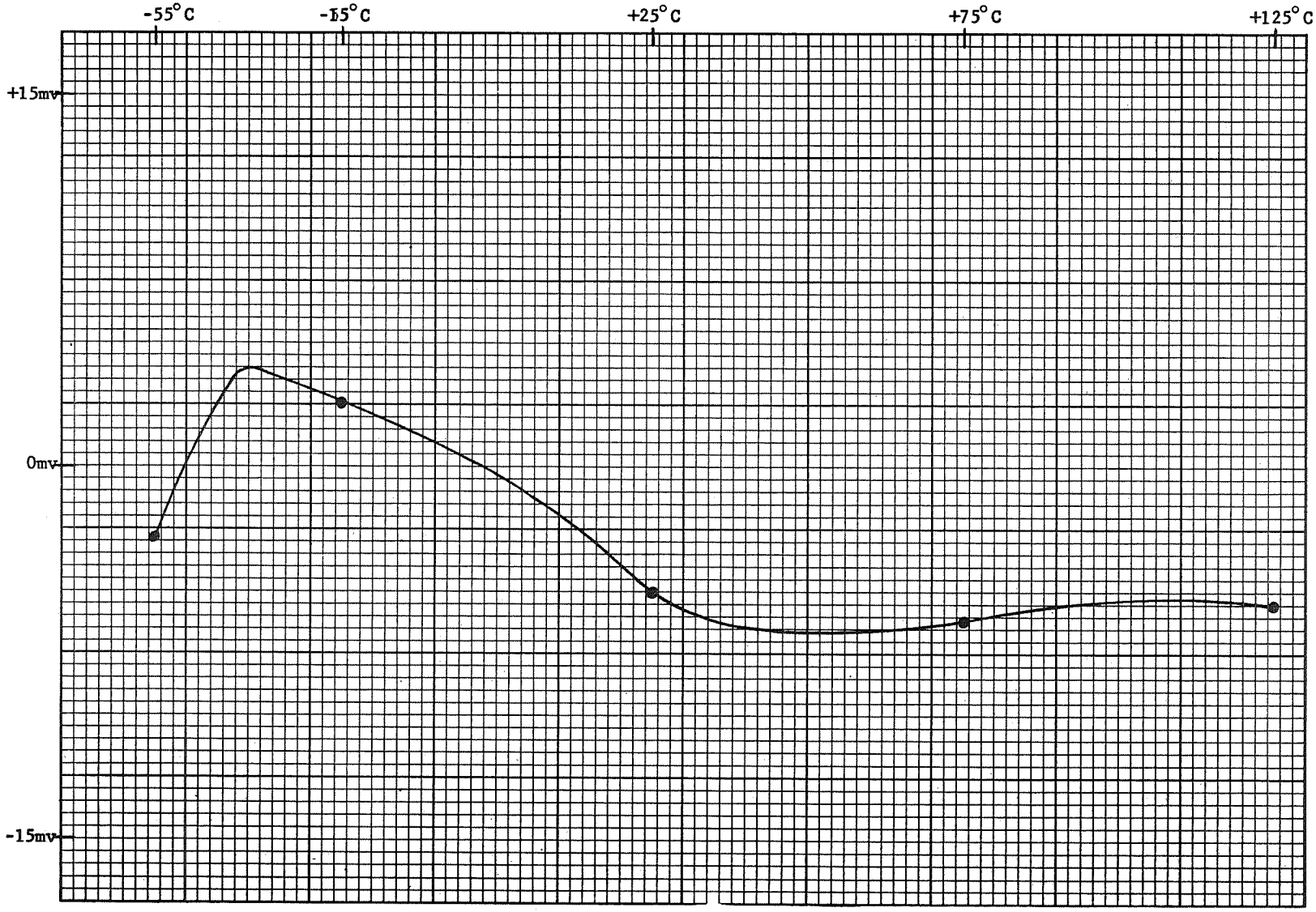

Figure 4-12b. Output Drift vs Temperature, Unit 54

MOA-10 TEST DATA

MODULE SERIAL NO: 51

DATE: 7-2-69 RUN: 15 WAFER: 42 DIE: 16

TEMPERATURE MEASUREMENTS

	Loop Gain AV_o	Output Swing with R_L = 5K Ω	Output Offset with Zero Input
+125°C			+7.7 mv
+ 75°C			+7.9 mv
+ 25°C	$3. \times 10^6$	6.8 V. P-P.	+ 5.4 mv
- 15°C			+ 1.7 mv
- 55°C			- 7.0 mv

ROOM TEMPERATURE MEASUREMENTS

Power Consumption: I_S = 1.2 ma, V_S = 4.5 V., $I_S \times V_S$ = 54 mw.

Output Resistance: V_o = 20. VRMS $\Delta V_o \geq$ < .01 VRMS $R_o = \frac{\Delta V_o}{0.6} \times 100$ = _____

V_o^1 = _____ $R_o < \frac{.01 \times 5100}{20} = 2.6\,\Omega$

Common-mode Rejection: ΔV_o(DM) = < .004 V. P-P CMR = $10 \times \frac{\Delta V_\phi(CM)}{\Delta V_{io}(DM)}$ ≥ 10,000

ΔV_i(CM) = .4 V P/P

Frequency Response: V_i = .100 VRMS V_o = 1.006 VRMS at 10 Hz, dB Attenuation = _____

V_i = .100 VRMS V_o = 1.026 VRMS at 2 KHz

Phase Shift: ϕ = _____ at 5 Hz

Figure 4-13a. Amplifier 51 Test Data

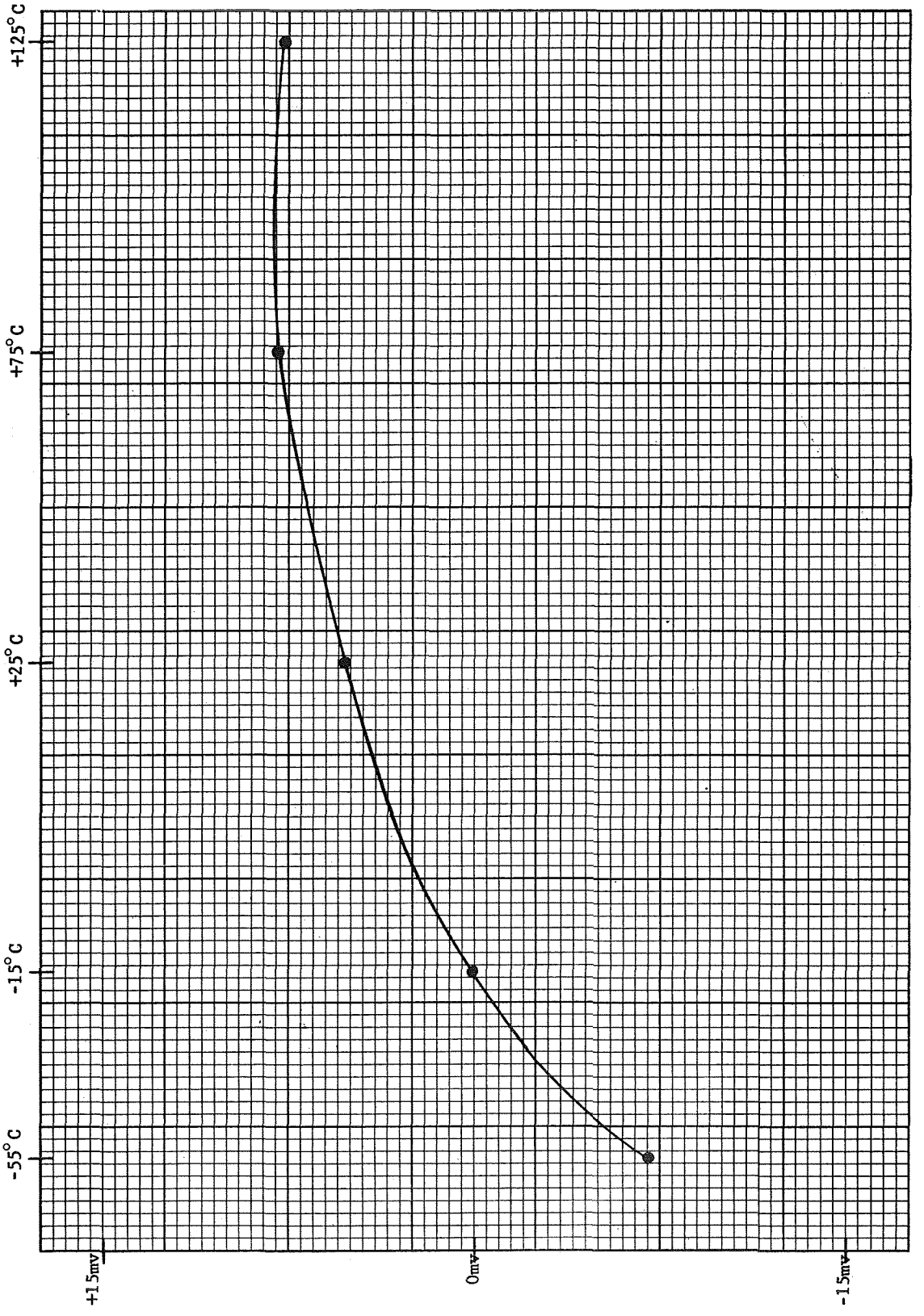

Figure 4-13b. Output Drift vs Temperature, Unit 51

MOA-10 TEST DATA

MODULE SERIAL NO: 101

DATE: 7-13-69 INPUT 29 RUN: 18 9 WAFER: 51 23 DIE: 6

TEMPERATURE MEASUREMENTS

	Loop Gain AV_o	Output Swing with R_L = 5K Ω	Output Offset with Zero Input
+125°C	3×10^6		-5.9 mV
+ 75°C	4×10^6		- 2.6 mV
+ 25°C	5×10^6	78.8V P-P	+ .5mV
- 15°C	3×10^6		+ 2.1 mV
- 55°C	2.4×10^6		- 2.3 mV

ROOM TEMPERATURE MEASUREMENTS

Power Consumption: I_S = .85ma, V_S = 45 VDC, $I_S \times V_S$ = 39 mW

Output Resistance: V_o = 20 VRMS, ΔV_o < .01 VRMS, $R_o = \frac{\Delta V_o}{0.6} \times 100$ = _____

V_o^1 = _____ $R_o < \frac{.01 \times 5100}{20} = 2.6\Omega$

Common-mode Rejection: ΔV_o(DM) = .004 VP/P, CMR = $10 \times \frac{\Delta V_\phi (CM)}{\Delta V_\phi (DM)}$ > 10,000

ΔV_i(CM) = 4 VP/P

Frequency Response: V_i = .100 VRMS V_o = 1.017 VRMS at 10 Hz, dB Attenuation = _____

V_i = .100 VRMS V_o = 1.021 VRMS at 2 KHz

Phase Shift: ϕ = _____ at 5 Hz

Figure 4-14a. Amplifier 101 Test Data

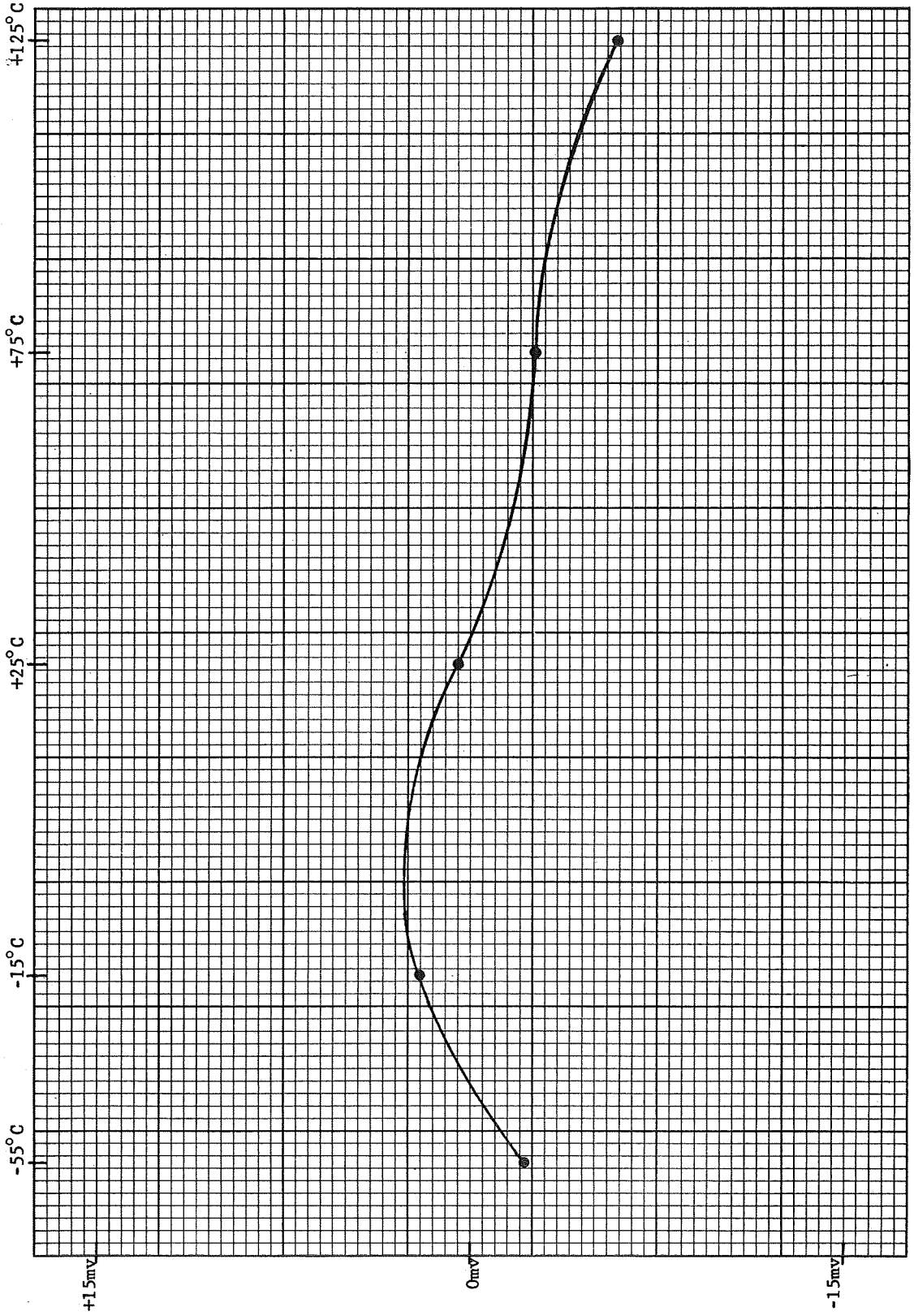

Figure 4-14b. Output Drift vs Temperature, Unit 101

MOA-10 TEST DATA

MODULE SERIAL NO: 117

DATE: 7-15-69 RUN: INPUT 26 / OUTPUT 26 WAFER: 7 DIE: 31 26

TEMPERATURE MEASUREMENTS

	Loop Gain AV_o	Output Swing with R_L = 5K Ω	Output Offset with Zero Input
+125°C			+6.0 mv
+ 75°C			+2.6 mv
+ 25°C	1.5×10^6	65.1 VP-P	+ .1 mV
- 15°C			-6.3 mV
- 55°C			+ 6.3 mV

ROOM TEMPERATURE MEASUREMENTS

Power Consumption: I_S = 1.1 ma, V_S = 45 VDC, $I_S \times V_S$ = 49.5 mw

Output Resistance: V_o = 20 VRMS ΔV_o < .01 VRMS, $R_o = \frac{\Delta V_o}{0.6} \times 100$ = _____

V_o^1 = _____ $R_o < \frac{.01 \times 5100}{20} = 2.6\ \Omega$

Common-mode Rejection: ΔV_o(DM) < .004 V P-P CMR = $10 \times \frac{\Delta V_o(CM)}{\Delta V_i(DM)}$ > 10,000

ΔV_i(CM) = 4 V. P-P

Frequency Response: V_i = .100 VRMS V_o = 1.005 VRMS at 10 Hz, dB Attenuation = _____

V_i = .100 VRMS V_o = 1.024 VRMS at 2 KHz

Phase Shift: ϕ = _____ at 5 Hz

Figure 4-15a. Amplifier 117 Test Data

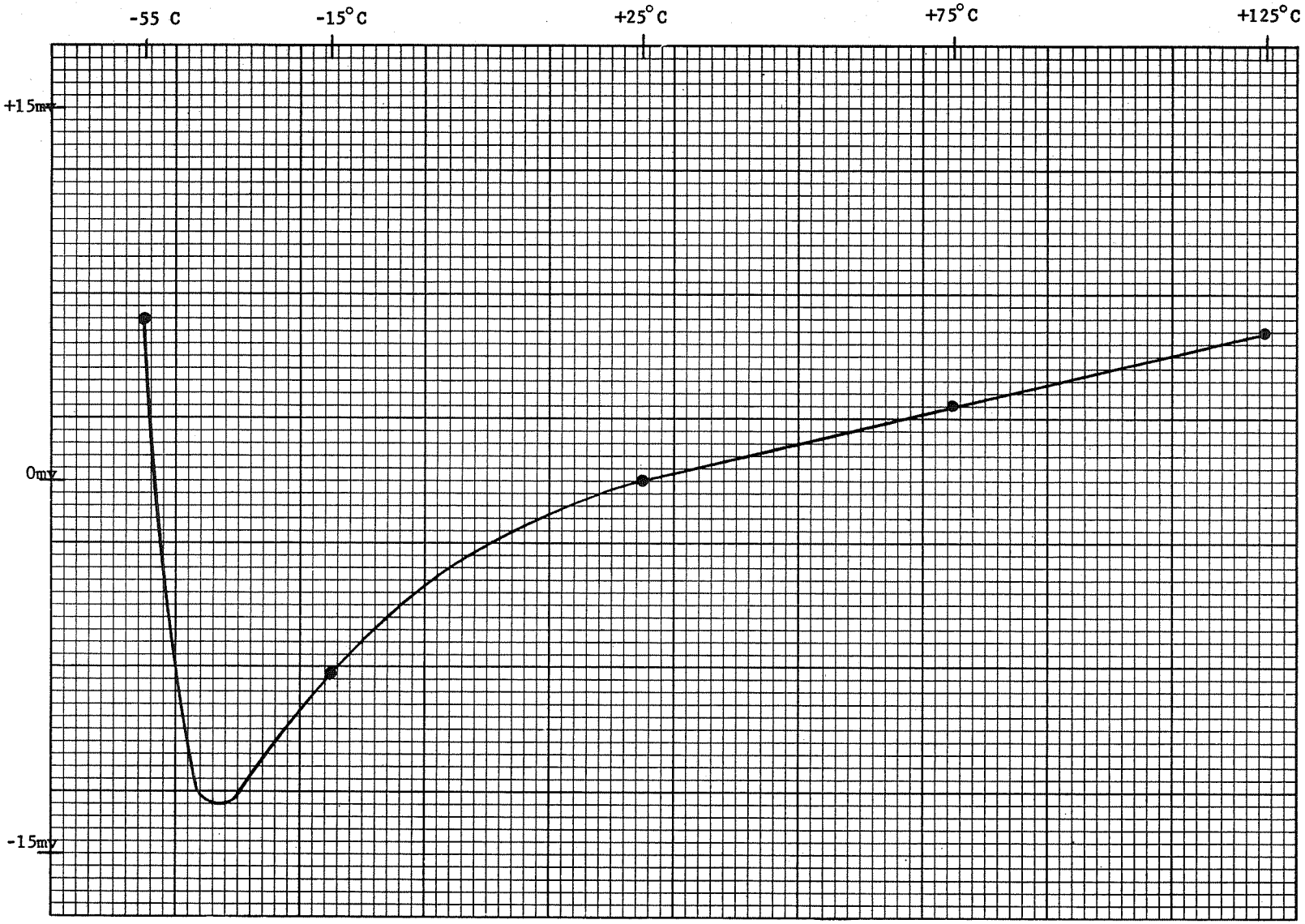

Figure 4-15b. Output Drift vs Temperature, Unit 117

MOA-10 TEST DATA

MODULE SERIAL NO: 72

DATE: 15 JULY 1969 RUN: 21 WAFER: 58 DIE: 16

TEMPERATURE MEASUREMENTS

	Loop Gain AV_o	Output Swing with R_L = 5K Ω	Output Offset with Zero Input
+125°C	2.0×10^6		+ 7.6 mV
+ 75°C	3.0×10^6		+ 4.9 mV
+ 25°C	3.0×10^6	60.3 V P-P	- .5 mV
- 15°C	2.3×10^6		- 6.0 mV
- 55°C	$.6 \times 10^6$		- 7.1 mV

ROOM TEMPERATURE MEASUREMENTS

Power Consumption: I_S = 12 ma, V_S = 45 VDC, $I_S \times V_S$ = 54 mW

Output Resistance: V_o = 20 VRMS, ΔV_o < .01 VRMS, $R_o = \frac{\Delta V_o}{0.6} \times 100$ = _____

V_o^1 = _____ $R_o < \frac{.01 \times 5100}{20.} = 2.6\ \Omega$

@ 10 Hz Common-mode Rejection: $\Delta V_o(DM)$ < .004 VP/P, $CMR = 10 \times \frac{\Delta V_o(CM)}{\Delta V_i(DM)}$ > 10,000

$\Delta V_i(CM)$ = 4 VP/P

Frequency Response: V_i = .100 VRMS V_o = 1.006 VRMS at 10 Hz, dB Attenuation = _____

V_i = .100 VRMS V_o = 1.041 VRMS at 2 KHz

Phase Shift: ϕ = _____ at 5 Hz

Figure 4-16a. Amplifier 72 Test Data

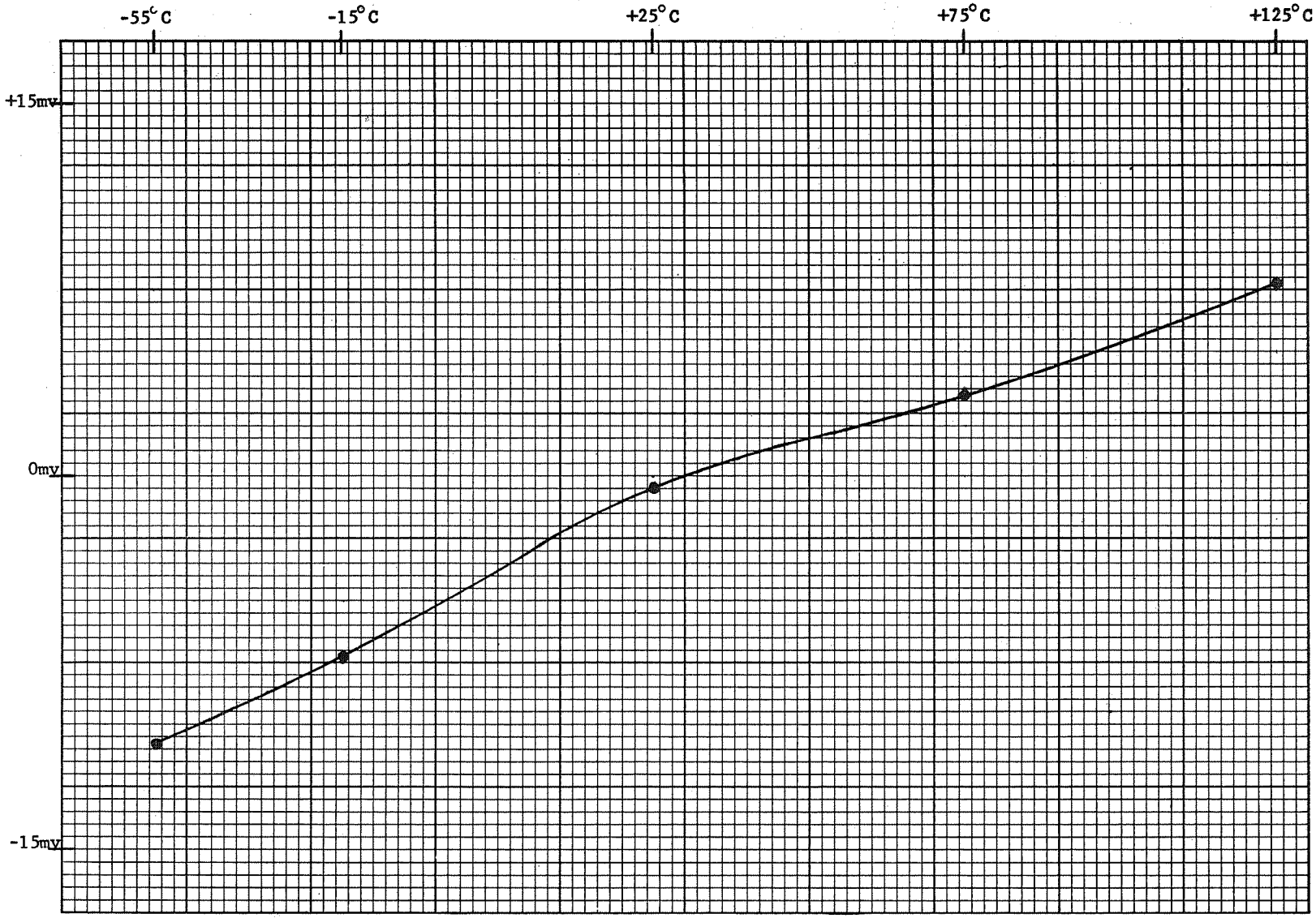

Figure 4-16b. Output Drift vs Temperature, Unit 72

MOA-10 TEST DATA

MODULE SERIAL NO: 60

DATE: 7-13-69 RUN: 21 WAFER: 59 DIE: 29

TEMPERATURE MEASUREMENTS

	Loop Gain AV_o	Output Swing with R_L = 5K Ω	Output Offset with Zero Input
+125°C	2.5 X 10^6		-4.2 mV
+ 75°C	3.5 X 10^6		-4.0 mV
+ 25°C	5.0 X 10^6	64 V.P-P	-5.2 mV
- 15°C	4.0 X 10^6		-4.0 mV
- 55°C	3.0 X 10^6		± 11.2 mV

ROOM TEMPERATURE MEASUREMENTS

Power Consumption: I_S = 1.1 ma, V_S = 45 VDC, $I_S \times V_S$ = 49.5 mW

Output Resistance: V_o = 20 VRMS, ΔV_o < .01 VRMS, $R_o = \frac{\Delta V_o}{0.6} \times 100$ = _____

V_o^1 = _____ $R_o < \frac{.01 \times 5100}{20} = 2.6\,\Omega$

Common-mode Rejection: ΔV_o(DM) < .004 VP/P, CMR = $10 \times \frac{\Delta V_i(CM)}{\Delta V_o(DM)}$ > 10,000

ΔV_i(CM) = 4 VP/P

Frequency Response: V_i = .100 VRMS V_o = 1.008 VRMS at 10 Hz, dB Attenuation = _____

V_i = .100 VRMS V_o = 1.007 VRMS at 2 KHz

Phase Shift: Ø = _____ at 5 Hz

Figure 4-17a. Amplifier 60 Test Data

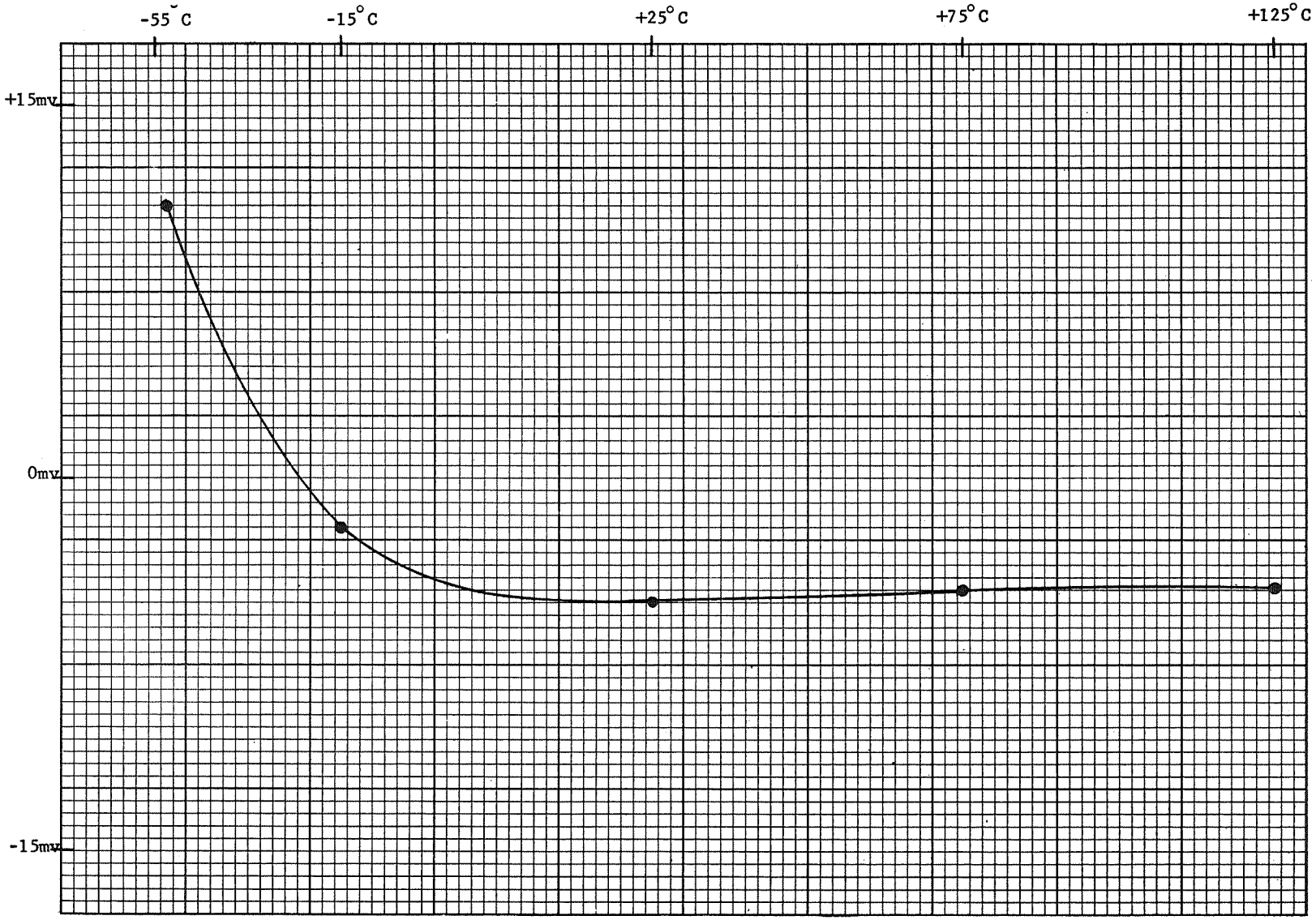

Figure 4-17b. Output Drift vs Temperature, Unit 60

MOA-10 TEST DATA

MODULE SERIAL NO: 58

DATE: 2JULY RUN: 21 WAFER: 59 DIE: 10

TEMPERATURE MEASUREMENTS

	Loop Gain AV_o	Output Swing with R_L = 5K Ω	Output Offset with Zero Input
+125°C			+5.6mv
+ 75°C			+3.2mv
+ 25°C	2.5×10^6	78VP/P	-0.5mv
- 15°C			-1.5mv
- 55°C			+13.5

ROOM TEMPERATURE MEASUREMENTS

Power Consumption: I_S = 1.05MA, V_S = 45VDC, $I_S \times V_S$ = 47.3mw

Output Resistance: V_o = 20VRMS, ΔV_o < .01VRMS, $R_o = \frac{\Delta V_o}{0.6} \times 100$ = _____

V_o^1 = _____ $R_o < \frac{.01 \times 5100}{20.} = 2.5\Omega$

Common-mode Rejection: ΔV_o(DM) < .004 VP/P, CMR = $10 \times \frac{\Delta V_i(CM)}{\Delta V_o(DM)}$ > 10,000

ΔV_i(CM) = 4VP/P

Frequency Response: V_i = .100VRMS V_o = .1016 VRMS at 10 Hz, dB Attenuation = _____

V_i = .100VRMS V_o = 1.057VRMS at 2 KHz

Phase Shift: ϕ = _____ at 5 Hz

Figure 4-18a. Amplifier 58 Test Data

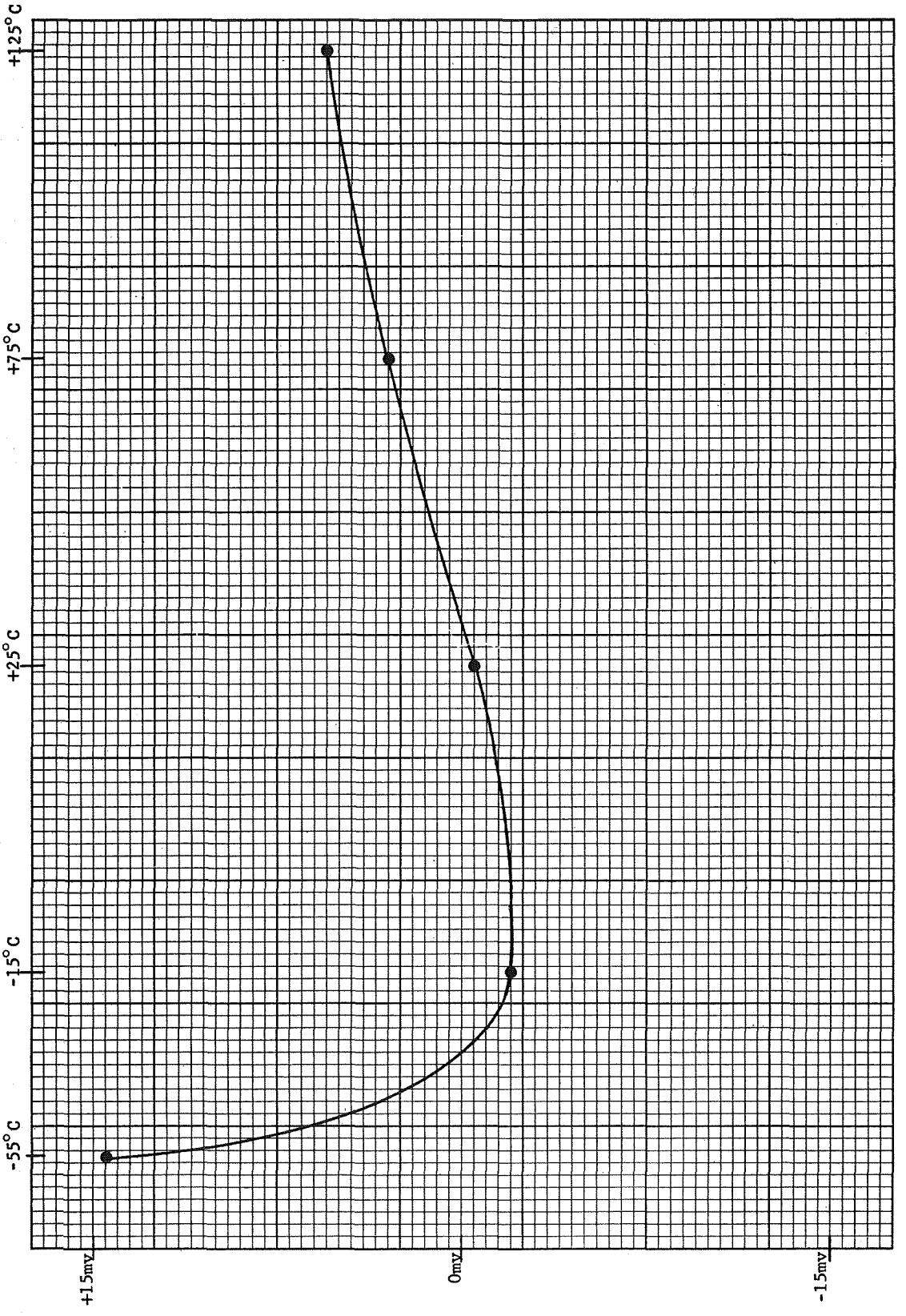

Figure 4-18b. Output Drift vs Temperature, Unit 58

MOA-10 TEST DATA

MODULE SERIAL NO: 50

DATE: 30 JUNE '69 RUN: 15 WAFER: 42 DIE: 13

TEMPERATURE MEASUREMENTS

	Loop Gain AV_o	Output Swing with R_L = 5K Ω	Output Offset with Zero Input
+125°C			+10 mv
+ 75°C			8.5 mv
+ 25°C	3.5×10^6	65 VP/P	+7.9 mv
- 15°C			6.3 mv
- 55°C			-1.0 mv

ROOM TEMPERATURE MEASUREMENTS

Power Consumption: I_S = 1.53 ma, V_S = 45 VDC, $I_S \times V_S$ = 69.7 mw

Output Resistance: V_o = 20. VRMS, ΔV_o < .010 VRMS, $R_o = \frac{\Delta V_o}{0.6} \times 100$ = _____

$V_o{}^1$ = _____ $R_o < \frac{.010 \times 5100}{20.} = 2.6\Omega$

Common-mode Rejection: ΔV_o(DM) = .020 VP/P, CMR = $10 \times \frac{\Delta V_\phi (CM)}{\Delta V_0 (DM)}$ = 2000

ΔV_i(CM) = 4 VP/P

Frequency Response: V_i = .100 VRMS V_o = 1.018 VRMS at 10 Hz, dB Attenuation = _____

V_i = .100 VRMS V_o = 1.03 VRMS at 2 KHz

Phase Shift: ∅ = _____ at 5 Hz

Figure 4-19a. Amplifier 50 Test Data

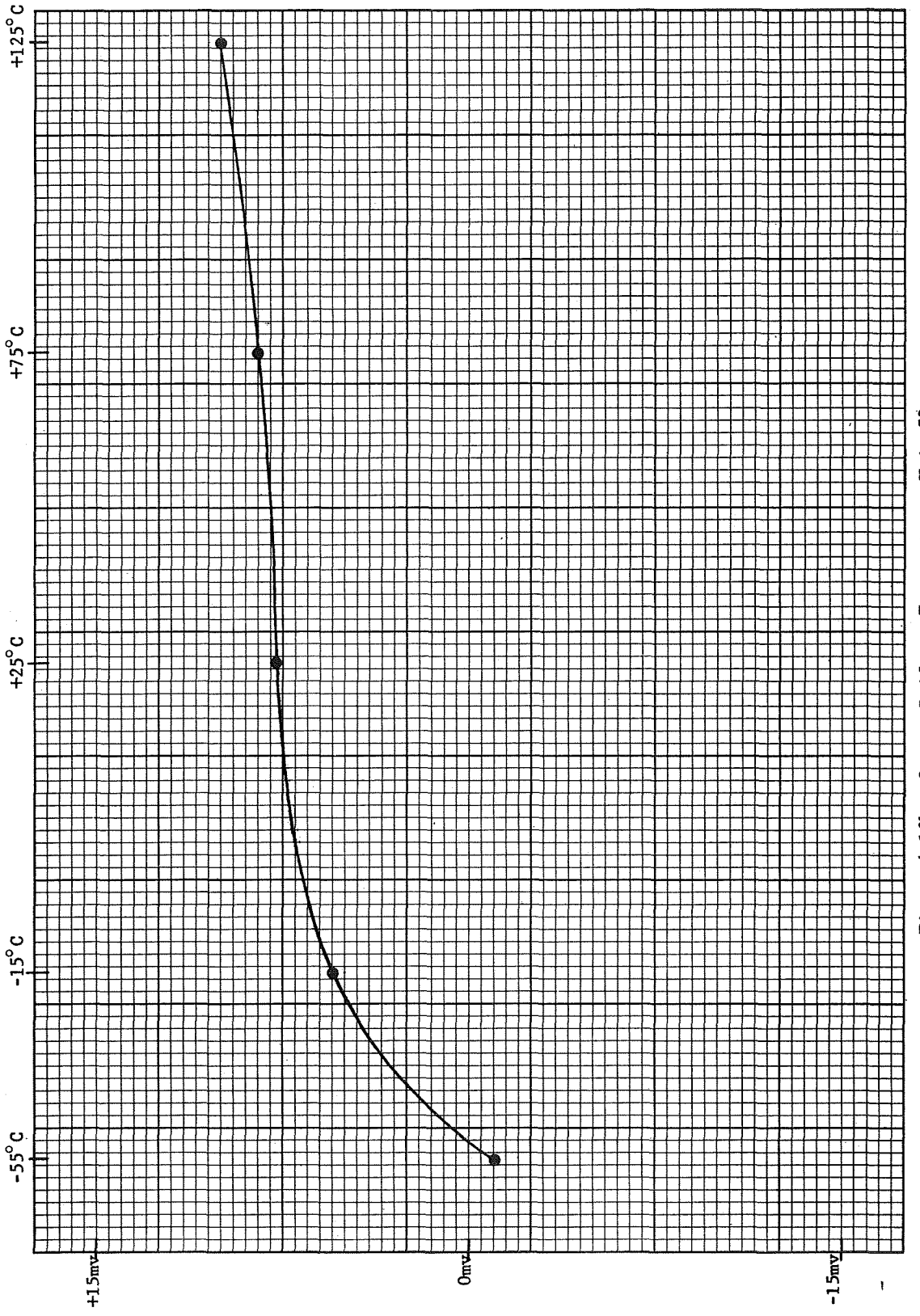

Figure 4-19b. Output Drift vs Temperature, Unit 50

MOA-10 TEST DATA

MODULE SERIAL NO: 102

DATE: 7-13-69 INPUT RUN: 25 26 WAFER: 6 8 DIE: 32 31

TEMPERATURE MEASUREMENTS

	Loop Gain AV_o	Output Swing with R_L = 5K Ω	Output Offset with Zero Input
+125°C	$.8 \times 10^6$		+4.0 mv
+ 75°C	1.3×10^6		+1.5 mv
+ 25°C	1.6×10^6	61.1 VP-P	-0.6 mv
- 15°C	1.8×10^6		-6.5 mv
- 55°C	1.2×10^6		-7.1 mv

ROOM TEMPERATURE MEASUREMENTS

Power Consumption: I_S = .89ma, V_S = 45VDC, $I_S \times V_S$ = 40mw

Output Resistance: V_o = 20VRMS, ΔV_o < .01VRMS, $R_o = \frac{\Delta V_o}{0.6} \times 100$ = _____

V_o^1 = _____ $R_o < \frac{.01 \times 5100}{20} = 2.6\Omega$

Common-mode Rejection: ΔV_o(DM) < .004VP/P, CMR = $10 \times \frac{\Delta V_i(CM)}{\Delta V_o(DM)}$ > 10,000

ΔV_i(CM) = 4VP/P

Frequency Response: V_i = .100VRMS V_o = 1.027VRMS at 10 Hz, dB Attenuation = _____

V_i = .100VRMS V_o = 1.053VRMS at 2 KHz

Phase Shift: ϕ = _____ at 5 Hz

Figure 4-20a. Amplifier 102 Test Data

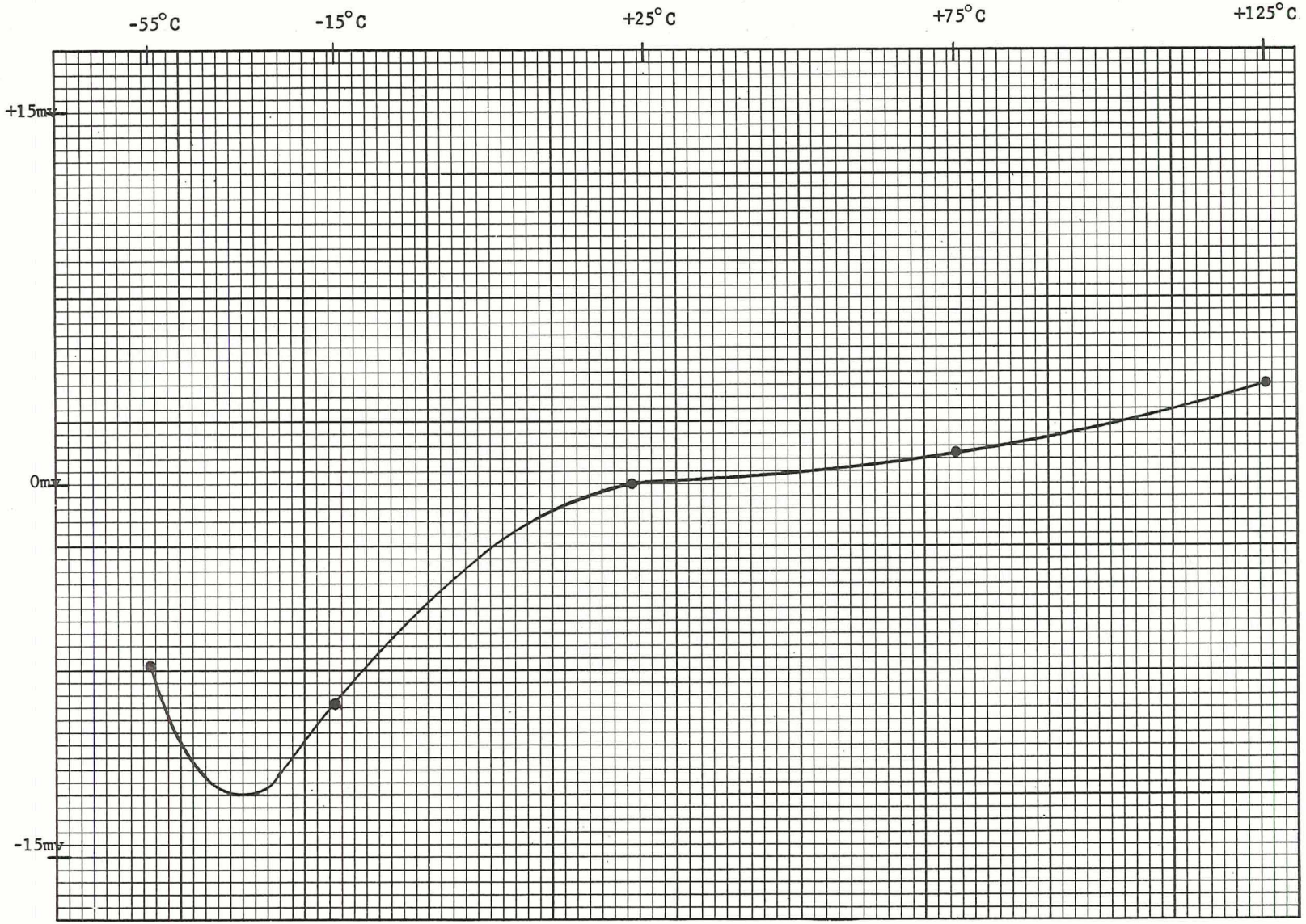

Figure 4-20b. Output Drift vs Temperature, Unit 102

MOA-10 TEST DATA

MODULE SERIAL NO: 62

DATE: 7-13-69 RUN: 15 WAFER: 46 DIE: 18

TEMPERATURE MEASUREMENTS

	Loop Gain AV_o	Output Swing with R_L = 5K Ω	Output Offset with Zero Input
+125°C	1.5×10^6		+14.3 mv
+ 75°C	2.2×10^6		+ 4.7mv
+ 25°C	2.6×10^6	62.4V P-P	- 7.0 mV
- 15°C	2.3×10^6		0.0 mv
- 55°C	1.4×10^6		+12.8 mv

ROOM TEMPERATURE MEASUREMENTS

Power Consumption: I_S = .52 ma, V_S = 45 VDC, $I_S \times V_S$ = 23.4 mw

Output Resistance: V_o = 20 VRMS, ΔV_o < .01 VRMS, $R_o = \frac{\Delta V_o}{0.6} \times 100$ = _____

V_o^1 = _____ $R_o < \frac{.01 \times 5100}{20} = 2.6\,\Omega$

Common-mode Rejection: ΔV_o(DM) < .004 VP/P, CMR = $10 \times \frac{\Delta V_i(CM)}{\Delta V_o(DM)}$ > 10,000

ΔV_i(CM) = 4 VP/P

Frequency Response: V_i = .100 VRMS V_o = 1.030 VRMS at 10 Hz, dB Attenuation = _____

V_i = .100 VRMS V_o = 1.091 VRMS at 2 KHz

Phase Shift: ϕ = _____ at 5 Hz

Figure 4-21a. Amplifier 62 Test Data

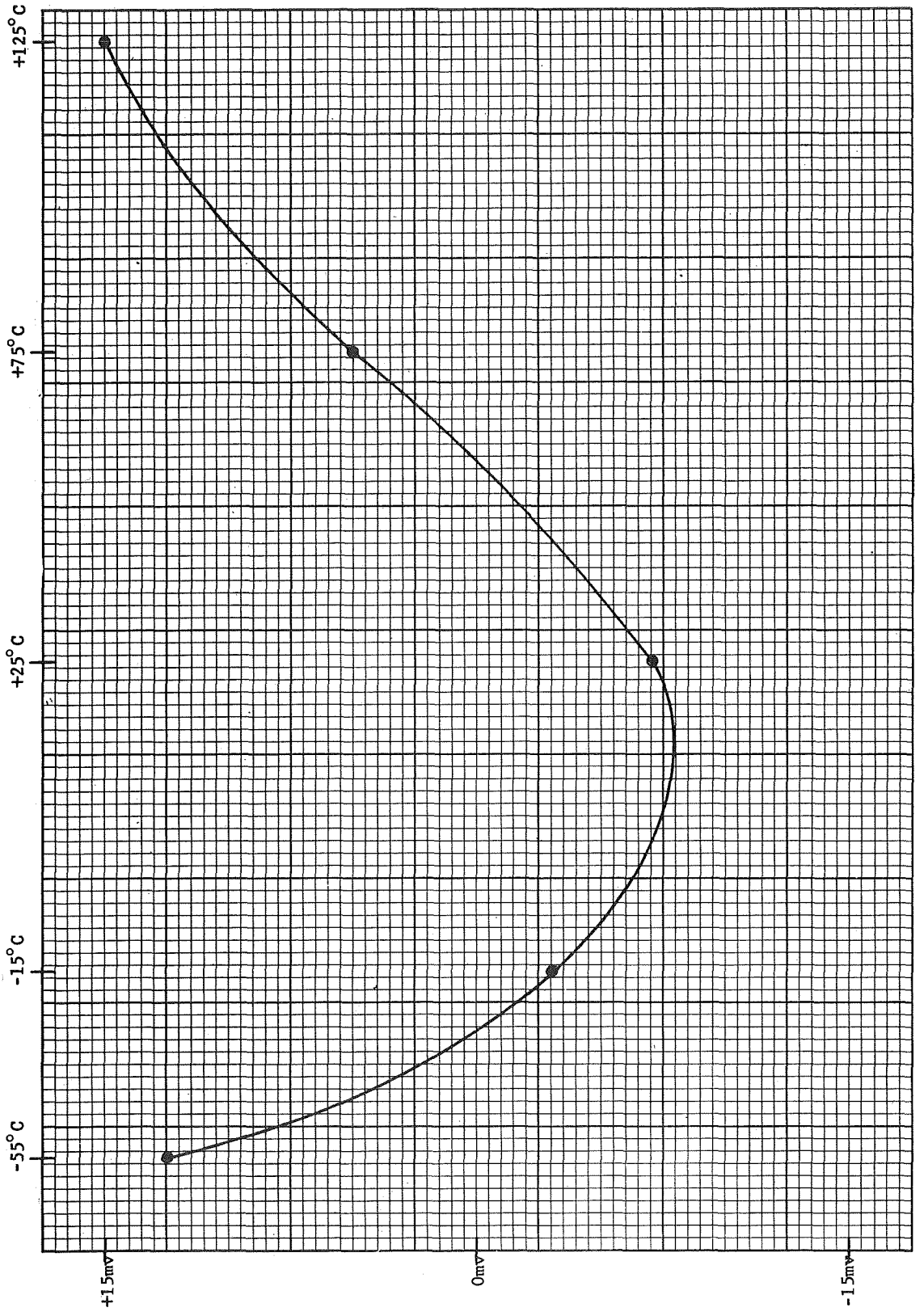

Figure 4-21b. Output Drift vs Temperature, Unit 62

MOA-10 TEST DATA

MODULE SERIAL NO: 59

DATE: 7-13-69 RUN: 21 WAFER: 59 DIE: 17

TEMPERATURE MEASUREMENTS

	Loop Gain AV_o	Output Swing with R_L = 5K Ω	Output Offset with Zero Input
+125°C	2.4×10^6		+3.9mv
+ 75°C	3.0×10^6		+4.5mv
+ 25°C	3.2×10^6	67.2 V P-P	-.9mv
- 15°C	3.0×10^6		-11.0mv
- 55°C	1.5×10^6		+15.0mv

ROOM TEMPERATURE MEASUREMENTS

Power Consumption: I_S = 1.1ma, V_S = 45Vdc, $I_S \times V_S$ = 49.5mw

Output Resistance: V_o = 20VRms, ΔV_o < .01VRMS, $R_o = \frac{\Delta V_o}{0.6} \times 100$ = _____

V_o^1 = _____ $R_o < \frac{.01 \times 5100}{50} = 2.6\Omega$

Common-mode Rejection: ΔV_o(DM) < .004VP/P, CMR = $10 \times \frac{\Delta V_i(CM)}{\Delta V_o(DM)}$ > 10,000

ΔV_i(CM) = 4 VP/P

Frequency Response: V_i = 1.00 VRMS V_o = 1.022 VRMS at 10 Hz, dB Attenuation = _____

V_i = 1.00 VRMS V_o = 1.025 VRMS at 2 KHz

Phase Shift: Ø = _____ at 5 Hz

Figure 4-22a. Amplifier 59 Test Data

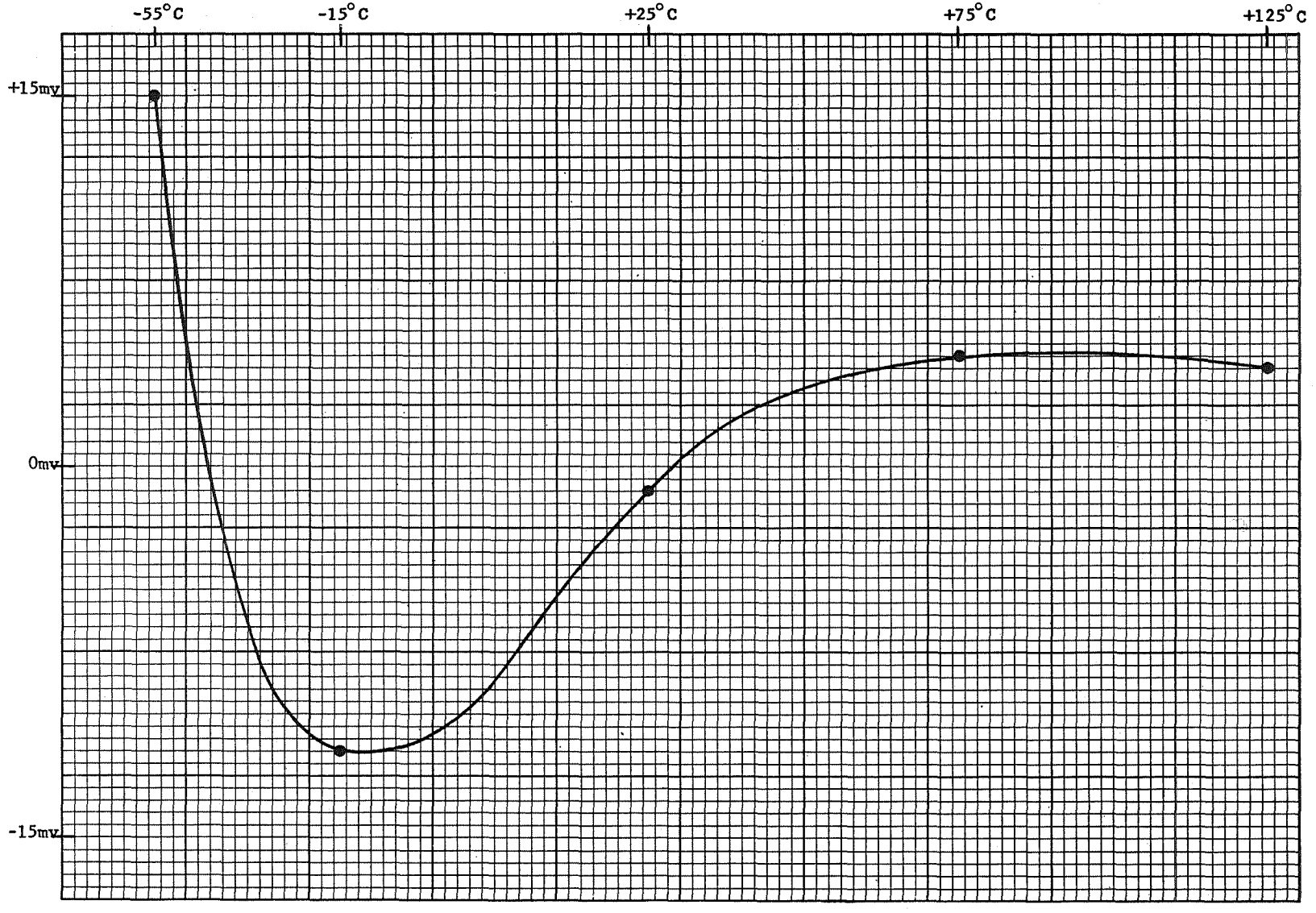

Figure 4-22b. Output Drift vs Temperature, Unit 59

MOA-10 TEST DATA

MODULE SERIAL NO: 57

DATE: 2 JULY 1969 RUN: 21 WAFER: 59 DIE: 9

TEMPERATURE MEASUREMENTS

	Loop Gain AV_o	Output Swing with R_L = 5K Ω	Output Offset with Zero Input
+125°C			+1.5 mv
+ 75°C			+3.4 mv
+ 25°C	2.0×10^6	60 VP/P	4.8 mv
- 15°C			+6.5
- 55°C			-10.6 mv

ROOM TEMPERATURE MEASUREMENTS

Power Consumption: I_S = 1.0 ma, V_S = 45 VDC, $I_S \times V_S$ = 45 mw

Output Resistance: V_o = 20 VRMS, ΔV_o < .01 VRMS, $R_o = \frac{\Delta V_o}{0.6} \times 100$ = _____

V_o^1 = _____ $R_o < \frac{.01 \times 5100}{20} = 2.5\ \Omega$

Common-mode Rejection: ΔV_o(DM) = .005 VP/P, CMR = $10 \times \frac{\Delta V_i(CM)}{\Delta V_o(DM)}$ = 8000

ΔV_i(CM) = 4 VP/P

Frequency Response: V_i = .100 VRMS V_o = 1.021 VRMS at 10 Hz, dB Attenuation = 0

V_i = .100 VRMS V_o = 1.057 VRMS at 2 KHz

Phase Shift: ϕ = _____ at 5 Hz

Figure 4-23a. Amplifier 57 Test Data

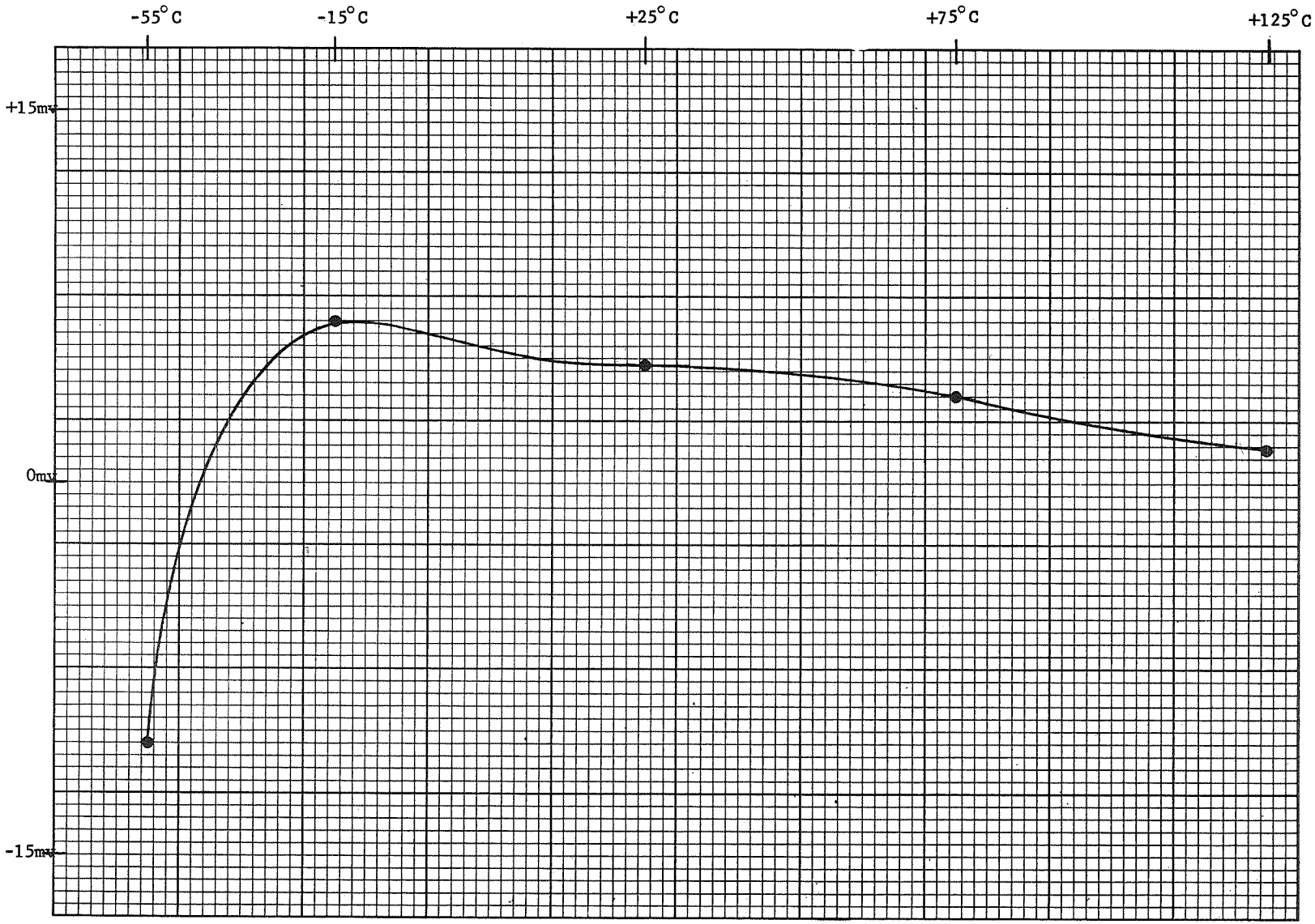

Figure 4-23b. Output Drift vs Temperature, Unit 57

MOA-10 TEST DATA

MODULE SERIAL NO: 27

DATE: 30 JUNE 1969 RUN: 26 WAFER: 8 DIE: 32

TEMPERATURE MEASUREMENTS

	Loop Gain AV_o	Output Swing with R_L = 5K Ω	Output Offset with Zero Input
+125°C			-14.4 mv
+ 75°C			-3.5 mv
+ 25°C	2.0×10^6	62 VP/P	+2.0 mv
- 15°C			+2.5 mv
- 55°C			+16 mv

ROOM TEMPERATURE MEASUREMENTS

Power Consumption: I_S = .67 mA, V_S = 45 VDC, $I_S \times V_S$ = 30 mw

Output Resistance: V_o = 20. VRMS, ΔV_o < .010 VRMS, ~~$R_o = \frac{\Delta V_o}{0.6} \times 100$~~ = _____

V_o^1 = _____ $R_o < 2.5\Omega$

Common-mode Rejection: ΔV_o(DM) ≅ .02 VP/P, $CMR = 10 \times \frac{\Delta V_o(CM)}{\Delta V_i(DM)} \cong$ 2000

ΔV_i(CM) = 4 VP/P

Frequency Response: V_i = .100 VRMS V_o = 1.021 VRMS at 10 Hz, dB Attenuation = _____

V_i = .100 VRMS V_o = 1.077 VRMS at 2 KHz

Phase Shift: ∅ = _____ at 5 Hz

Figure 4-24a. Amplifier 27 Test Data

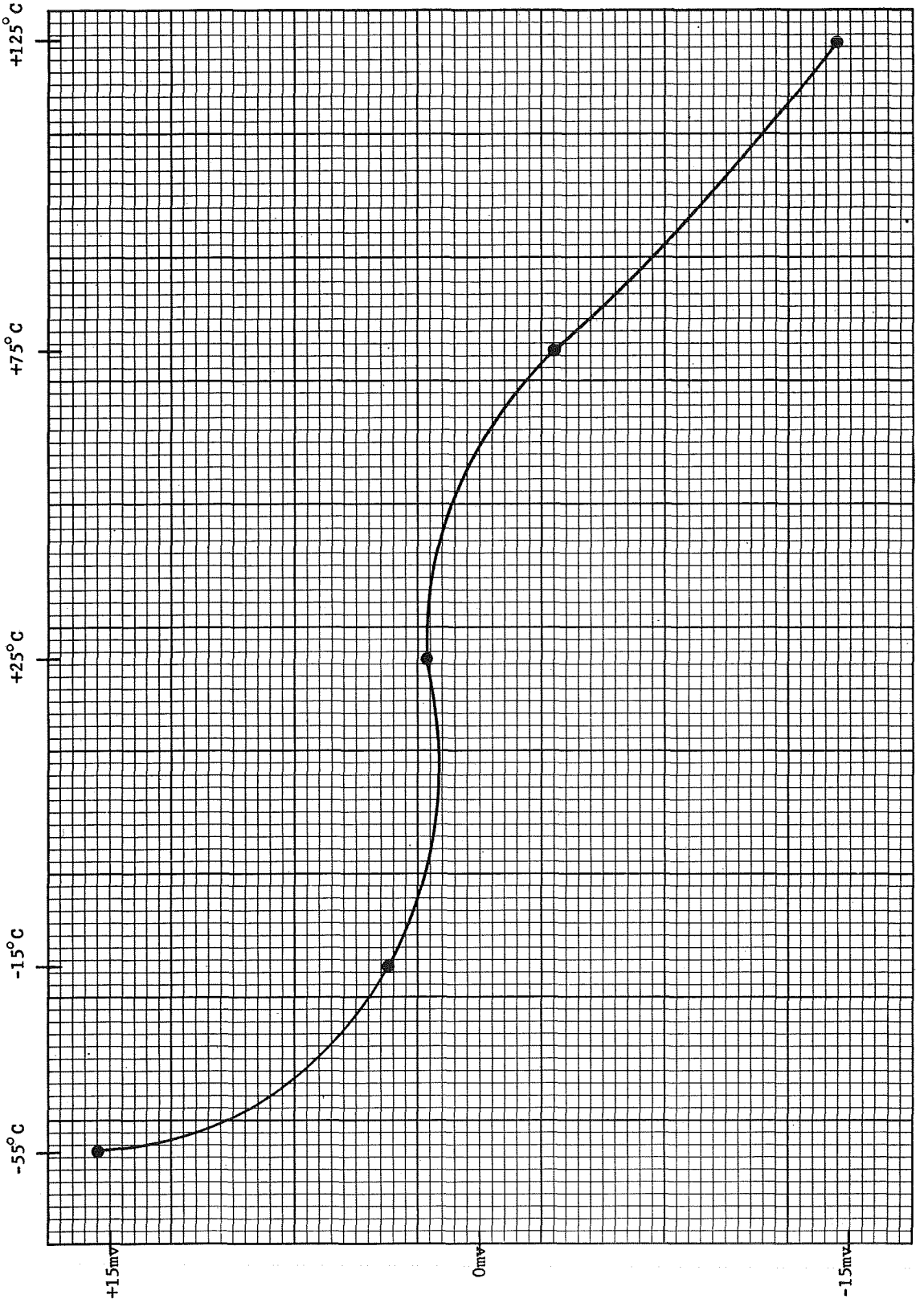

Figure 4-24b. Output Drift vs Temperature, Unit 27

MOA-10 TEST DATA

MODULE SERIAL NO: 38

DATE: 30 JUNE 1969 RUN: 2.5 WAFER: 6 DIE: 15

TEMPERATURE MEASUREMENTS

	Loop Gain AV_o	Output Swing with R_L = 5K Ω	Output Offset with Zero Input
+125°C			+4.5mv
+ 75°C			+0.7 mv
+ 25°C	1.1×10^6	66 VP/P	-5.4mv
- 15°C			13. mv
- 55°C			+18.5mv
-45			0 mv

ROOM TEMPERATURE MEASUREMENTS

Power Consumption: I_S = 0.75ma, V_S = 45VDC, $I_S \times V_S$ = 34mw

Output Resistance: V_o = 20.VRMS, ΔV_o < .010 VRMS, $R_o = \frac{\Delta V_o}{0.6} \times 100$ = _____

$V_o{}^1$ = _____ $R_o < \frac{.010 \times 5100}{20.} = 2.6\ \Omega$

Common-mode Rejection: ΔV_o(DM) = .035 VP/P, CMR = $10 \times \frac{\Delta V_o(CM)}{\Delta V_o(DM)}$ = 1100

ΔV_1(CM) = 4 VP/P

Frequency Response: V_i = .100VRMS V_o = 1.023 VRMS at 10 Hz, dB Attenuation = _____

V_i = .100 VRMS V_o = 1.034 VRMS at 2 KHz

Phase Shift: ϕ = _____ at 5 Hz

Figure 4-25a. Amplifier 38 Test Data

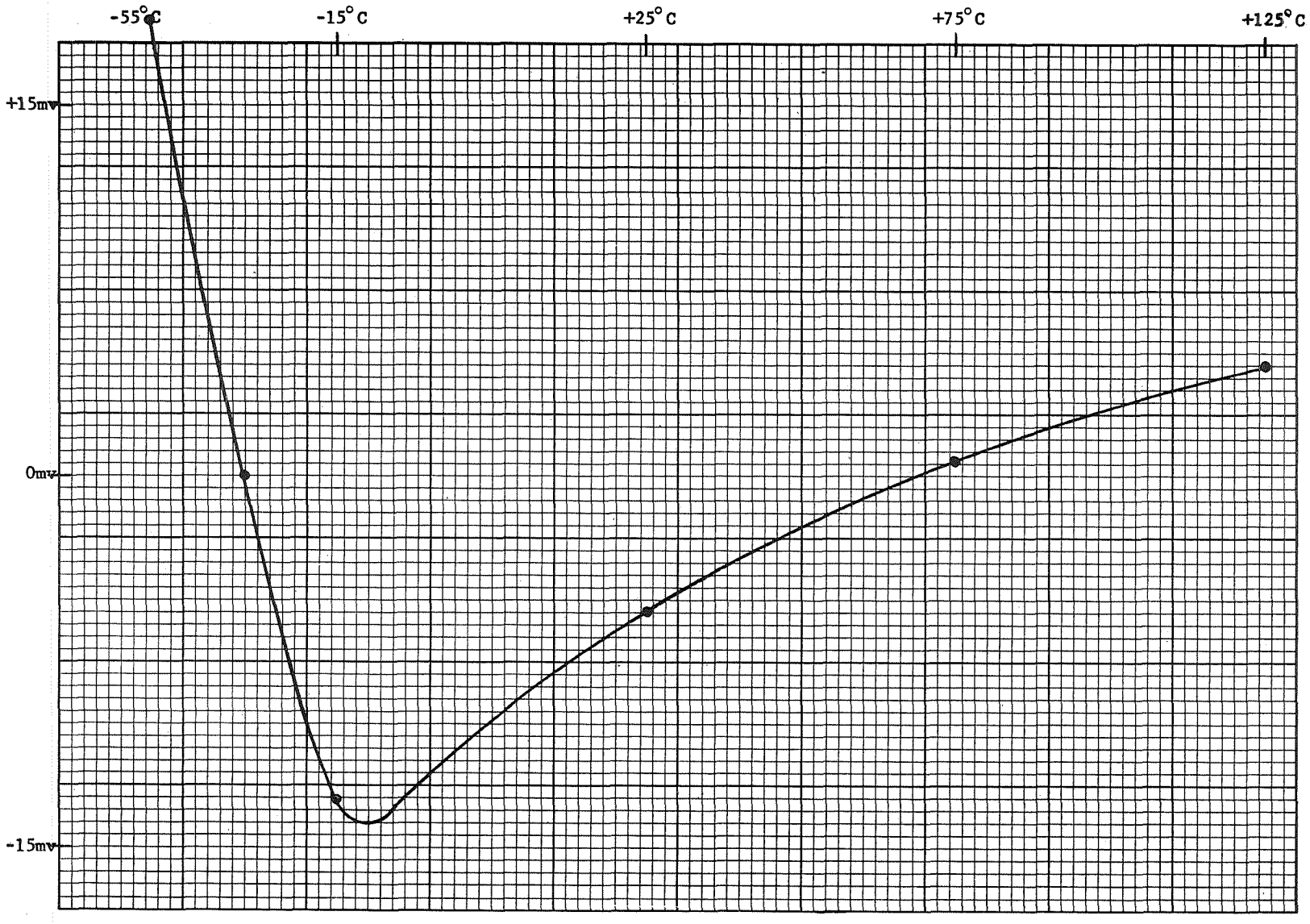

Figure 4-25b. Output Drift vs Temperature, Unit 38

Module	Max V_O Drift (+)	Max V_O Drift (-)	A_{VO}	ΔV_O	P_D	CMR	R_O	F_{CO}
41	+ 4.5 mv	- 7.5 mv	2.5×10^6	68 volt	45 mw	1,300	<2.6 Ω	>2 KHz
54	+ 1.0 mv	- 6.1 mv	2.8×10^6	66 volt	35 mw	10,000	<2.6 Ω	>2 KHz
51	+ 7.9 mv	- 7.0 mv	3.0×10^6	68 volt	54 mw	>10,000	<2.6 Ω	>2 KHz
101	+ 2.1 mv	- 5.9 mv	5.0×10^6	79 volt	39 mw	10,000	<2.6 Ω	>2 KHz
117	+ 6.3 mv	- 6.3 mv	1.5×10^6	65 volt	50 mw	>10,000	<2.6 Ω	>2 KHz
72	+ 7.6 mv	- 7.1 mv	3.0×10^6	60 volt	54 mw	>10,000	<2.6 Ω	>2 KHz
60	+11.2 mv	- 5.2 mv	5.0×10^6	64 volt	50 mw	>10,000	<2.6 Ω	>2 KHz
58	+13.5 mv	- 1.5 mv	2.5×10^6	78 volt	47 mw	>10,000	<2.6 Ω	>2 KHz
50	+10.0 mv	- 1.0 mv	3.5×10^6	65 volt	70 mw	2,000	<2.6 Ω	>2 KHz
102	+ 4.0 mv	- 7.1 mv	1.6×10^6	61 volt	40 mw	>10,000	<2.6 Ω	>2 KHz
62	+14.3 mv	- 7.0 mv	2.6×10^6	62 volt	23 mw	>10,000	<2.6 Ω	>2 KHz
59	+15.0 mv	- 7.1 mv	1.6×10^6	61 volt	40 mw	>10,000	<2.6 Ω	>2 KHz
57	+ 6.5 mv	-10.6 mv	2.0×10^6	60 volt	45 mw	8,000	<2.6 Ω	>2 KHz
27	+16.0 mv	-14.4 mv	2.0×10^6	62 volt	30 mw	2,000	<2.6 Ω	>2 KHz
38	+18.5 mv	- 5.4 mv	1.1×10^6	66 volt	34 mw	1,100	<2.6 Ω	>2 KHz

Figure 4.26. MOA-10 Summarized Test Data

Item	MOA - 10 Serial No.	Before			After Shock			After Vibration		
		Seal	A_{VO}	$\equiv V_{iO}$	Seal	A_{VO}	$\equiv V_{iO}$	Seal	A_{VO}	$\equiv V_{iO}$
1	25	1.5×10^{-8}	2×10^{6}	+2.6 mv	1.8×10^{-8}	2×10^{6}	+2.6 mv	3.0×10^{-8}	2.3×10^{6}	+2.6 mv
2	26	1.5×10^{-8}	2×10^{6}	-2.2 mv	2.0×10^{-8}	2×10^{6}	-2.1 mv	2.5×10^{-8}	2×10^{6}	-2.1 mv
3	64	1.5×10^{-8}	3×10^{6}	-2.0 mv	2.5×10^{-8}	3×10^{6}	-2.0 mv	2.5×10^{-8}	3×10^{6}	-1.9 mv
4	65	1.5×10^{-8}	3×10^{6}	- .6 mv	2.0×10^{-8}	3×10^{6}	- .6 mv	3.0×10^{-8}	3×10^{6}	- .5 mv
5	67	2.5×10^{-8}	3×10^{6}	-4.6 mv	4.0×10^{-8}	3×10^{6}	-4.5 mv	1.0×10^{-7}	3×10^{6}	-4.5 mv
6	33	2.0×10^{-8}	1.4×10^{6}	-1.2 mv	2.5×10^{-8}	1.4×10^{6}	-1.1 mv	3.2×10^{-8}	1.2×10^{6}	-1.1 mv
7	43	2.0×10^{-8}	1×10^{6}	- .3 mv	2.5×10^{-8}	1×10^{6}	- .2 mv	3.5×10^{-8}	1×10^{6}	- .3 mv
8	52	1.5×10^{-8}	2×10^{6}	-6.4 mv	3.0×10^{-8}	2×10^{6}	-6.4 mv	2.5×10^{-8}	2×10^{6}	-6.4 mv
9	69	1.5×10^{-8}	2.4×10^{6}	-4.1 mv	2.0×10^{-8}	3×10^{6}	-4.2 mv	2.5×10^{-8}	3×10^{6}	-4.2 mv
10	109	2.0×10^{-8}	2.8×10^{6}	-4.6 mv	2.0×10^{-8}	2.8×10^{6}	-4.6 mv	3.0×10^{-8}	2.6×10^{6}	-4.4 mv

Figure 4.27 Measured Data From Mechanical Testing

4.5 Evaluation

Examination of the test data from Figure 4.11 through Figure 4.26 shows that the MOA-10 amplifier is designed to and capable of meeting the specifications stated in Section 1.0. A review of the electrical performance with respect to circuit design, integrated circuit mask lay-out, and processing is, however, helpful in understanding the present producibility status of this circuit.

The BV_{ceo} breakdown voltages were more difficult to obtain than originally anticipated for the specified collector resistivity. This was probably due to surface effects peculiar to this dielectrically isolated circuit. To accommodate this difficulty the Beta spec was reduced, in some cases to as low as 40 at room temperature. Since Betas fall off to 50% nominal value at -55°C, low temperature circuit behavior should be properly interpreted. In the future, the collector resistivity should be specified higher, allowing the Beta and BV_{ceo} specifications to be met simultaneously.

The ±15 mv output offset versus temperature specification is obtainable, but examination of the drift shows that the largest errors are typically found at temperatures below -30°C. This is probably due to the effect of reduced transistor Betas at lower temperatures as previously noted. The unique technique of drift-offset adjustment has been demonstrated as quite effective, particularly between 0°C and +125°C, as shown by the typical drift-temperature linearity in that temperature range. It would therefore appear feasible to consider a much tighter specification for dc offset, say ±5 mv, if the temperature range could be modified.

Another factor worth noting is the time-temperature stability of the thin film resistors after laser adjustment. The more adjustment a resistor receives, the more bakeout time is required to stabilize the resistance value. This in turn requires a vernier trimming after bakeout. If more laser blowout links were included, the laser annealing adjustments could be kept to small increments, and the above effect reduced.

The open loop gain specification was not difficult to obtain. The low Beta problem, however, does affect gain at negative temperature. It is therefore assumed that the gains would consistently be greater than 2×10^6 for proper Beta values.

The 60 volt peak-to-peak output voltage swing is obtainable, but some of the units were uncomfortably close to this minimum specification. This is probably due to variations in the output common-mode voltage of the input section. This parameter is a function of the Beta match of the PNP devices in the 3rd stage bias network, Q_{6A}, Q_{6B}, and Q_{21}. If these Betas are mismatched, they can be compensated by laser resistor adjustments, a process which was not used on the initial circuits delivered.

The power dissipation, common-mode rejection, output impedance, frequency response, and phase-shift specification appear in good order.

There was one problem uncovered, however, which does demand attention prior to additional amplifier fabrication. This is a small oscillation which appears only in the loaded condition when an output is driven negative. This is independent of overall loop stability, and is attributed to the local feedback loop established by Q_{33}, Q_{34A}, and Q_{34B}. This

triplicate must be analyzed and restructured at the mask level to insure proper stability margins at all output and environmental conditions.

Also, the division of the die into two sections requires an unfavorable bonding sequence. To avoid the crossover of bonding wires, the metal mask should be modified. This is not recognized as a difficult task.

The mechanical testing of ten functional modules insures that the hermeticity and electrical performance is not substantially changed due to the specified shock and vibration tests.

5.0 SUMMARY AND CONCLUSIONS

The unique drift-offset control circuitry proved to be very effective. All major requirements of the MOA-10 were met including electrical and environmental specifications. They were:

Drift

Power Consumption

Output voltage swing

Open loop gain

Common-mode rejection

Output impedance

Freqency response

Phase shift

Temperature

Altitude

Shock

Vibration

Some items, identified in Section 4.5, do require attention if a follow-on fabrication cycle is initiated. Included are mask modifications to eliminate local oscillations in the negative output drive triplicate and a change in the metal interconnection to avoid wire bond crossovers. In addition, the collector resistivity would be specified higher.

In conclusion, an amplifier has been developed which meets the contract requirements.

APPENDIX A

The MOA-5 amplifier is shown in Figure A-1. The final part count is:

15 NPN transistors

10 PNP transistors

26 resistors

2350 K ohms - total nominal resistance

The monolithic circuit design includes vertical NPN's, vertical PNP devices with electrical design goals shown in Table A-1, physical data in Table A-2, and ac parameter data in Table A-3.

The process sequence used to form the n-type and p-type collector regions is shown in Figure A-2. P-type starting material, which later becomes the PNP collector, is lapped and cleaned. After an oxide is formed, holes are etched into the oxide and the silicon. N-type silicon, which later becomes the NPN collector, is then epitaxially deposited and the wafer lapped back to form separate n-type and p-type regions.

Collector isolation channels are etched, after another oxide growth, to leave n- and p-type collector islands. The oxide is removed and the wafer cleaned. A layer of molybdenum is then deposited over the n- and p-type collector islands to provide a low resistivity buried layer for both the NPN and PNP transistors without requiring separate n+ and p+ diffused buried layers in the NPN and PNP devices, respectively. This approach therefore requires a minimum number of process steps.

An oxide isolation layer is then deposited before the polycrystalline silicon is deposited. The p-type silicon is lapped back through the

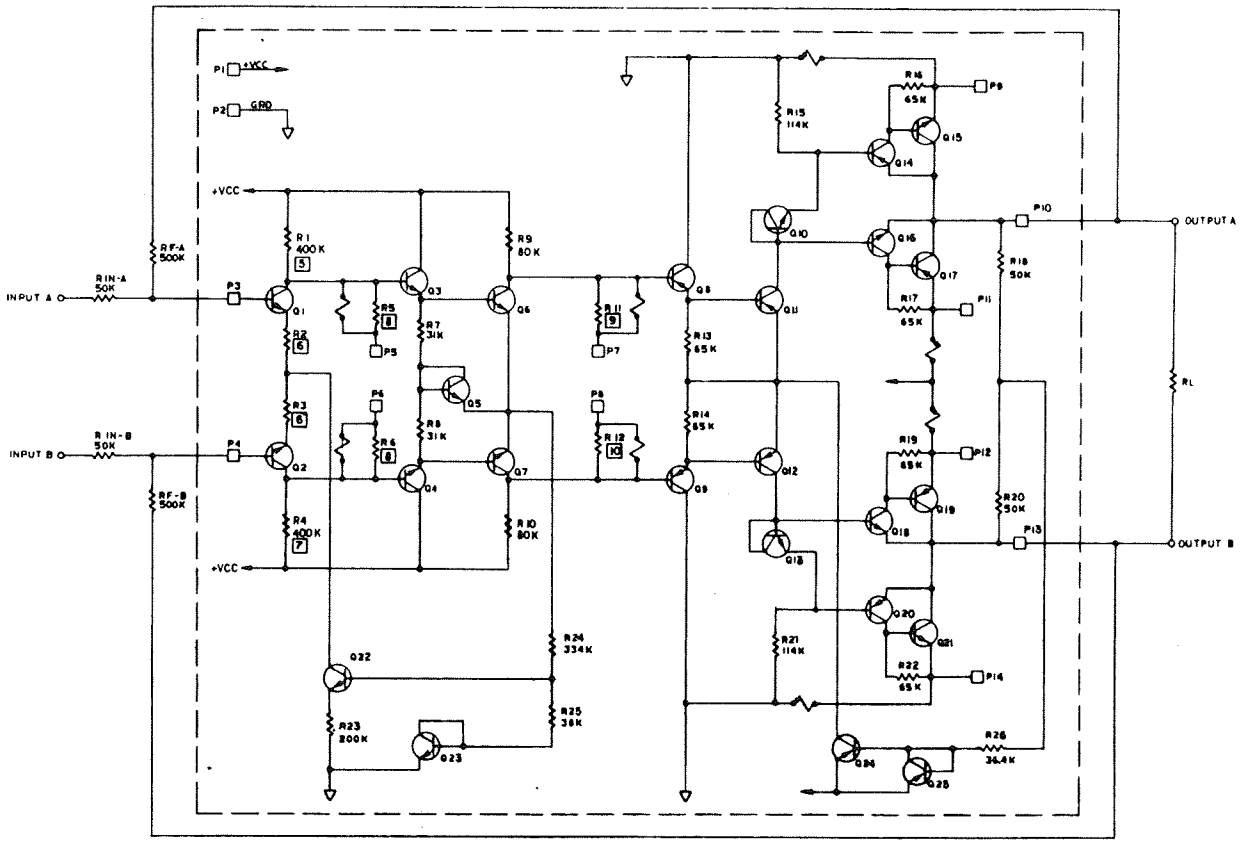

Figure A-1. **Monolithic Operational Amplifier Circuit Design (MOA5-1)**

TABLE A-1. TRANSISTOR DESIGN PARAMETERS

Parameter	NPN			PNP		
	Min.	Nom.	Max.	Min.	Nom.	Max.
$\beta \Big\vert_{I_c = 1\ mA}^{+25^oC}$	150	200	300	100	150	200
$\beta \Big\vert_{I_c = 10\mu A}^{+25^oC}$	100	150	200	70	100	150
$\beta \Big\vert_{I_c = 10\mu A}^{+125^oC}$	200	300	400	150	200	300
$\beta \Big\vert_{I_c = 10\mu A}^{-55^oC}$	50	70	100	35	50	70
BV_{CEO} (volts)	50			50		
r'_C (ohms)	100	200	300	300	450	600

TABLE A-2. **TRANSISTOR DATA**

Junction Areas	Minimum	Nominal	Maximum	
Collector-Substrate	37	50	62	$mils^2$
Base-Collector	6.6	7.6	8.7	$mils^2$
Emitter-Base	2.1	2.7	3.3	$mils^2$
Diffusion				
W_C' (collector depth)	22	27	32	microns
NPN - W_B'		2.5		microns
W_E'		1.5		microns
W_B	0.7	1.0	1.3	microns
ρ_c	3		5	ohm-cm
PNP - W_B'		2.7		microns
W_E'		1.5		microns
W_B	0.8	1.2	1.56	microns
ρ_c	8		12	ohm-cm

TABLE A-3. CALCULATED TRANSISTOR PARAMETERS

Parameter	NPN Min.	NPN Nom.	NPN Max.	PNP Min.	PNP Nom.	PNP Max.	Unit
C_{CB} at V_{CB} = 40V	.06	.08	.10	.04	.07	.10	pF
= 20V	.09	.11	.14	.06	.10	.13	pF
= 10V	.12	.15	.19	.12	.15	.18	pF
= 4V	.18	.24	.30	.18	.24	.29	pF
= 1V	.36	.48	.60	.34	.45	.57	pF
C_{TE}	2.1	2.7	3.4	2.1	2.7	3.4	pF
C_{CS}	.64	1.0	1.3	.64	1.0	1.3	pF
ω_E^{-1} at I_c = 2.5μA	2.2×10^{-8}	2.8×10^{-8}	3.5×10^{-8}	2.2×10^{-8}	2.8×10^{-8}	3.5×10^{-8}	sec.
= 10μa	5.5×10^{-9}	7.0×10^{-9}	8.8×10^{-9}	5.5×10^{-9}	7.0×10^{-9}	8.8×10^{-8}	sec.
= 50μA	1.1×10^{-9}	1.4×10^{-9}	1.8×10^{-9}	1.1×10^{-9}	1.4×10^{-9}	1.8×10^{-9}	sec.
= 200μA	2.7×10^{-10}	3.5×10^{-10}	4.4×10^{-10}	2.7×10^{-10}	3.5×10^{-10}	4.4×10^{-10}	sec.
= 1 mA	5.5×10^{-11}	7.0×10^{-11}	8.8×10^{-11}	5.5×10^{-11}	7.0×10^{-11}	8.8×10^{-11}	sec.
ω_α^{-1}	3.3×10^{-11}	6.7×10^{-11}	11×10^{-11}	1.3×10^{-10}	2.9×10^{-10}	4.9×10^{-10}	sec.
ω_C^{-1} at V_{CB} = 40V	6×10^{-12}	16×10^{-12}	30×10^{-12}	12×10^{-12}	31×10^{-12}	60×10^{-12}	sec.
= 20V	9×10^{-12}	24×10^{-12}	42×10^{-12}	18×10^{-12}	45×10^{-12}	78×10^{-12}	sec.
= 10V	12×10^{-12}	32×10^{-12}	57×10^{-12}	36×10^{-12}	68×10^{-12}	108×10^{-12}	sec.
= 4V	18×10^{-12}	48×10^{-12}	90×10^{-12}	54×10^{-12}	108×10^{-12}	172×10^{-12}	sec.
= 1V	36×10^{-12}	96×10^{-12}	180×10^{-12}	102×10^{-12}	200×10^{-12}	342×10^{-12}	sec.
f_T - Q_1	12.7	16.0	20.5	MHz at I_c = 10μA,	V_{CB} = 20 volts		
- Q_2	3.2	4.1	5.2	MHz at I_c = 2.5μA,	V_{CB} = 4 volts		
- Q_6	48	64	96	MHz at I_c = 50μA,	V_{CB} = 1 volt		
- Q_8	at I_c = 10 μA, V_{CB} = 40 volts			12	13	20	MHz
- Q_{11}				112	164	270	MHz

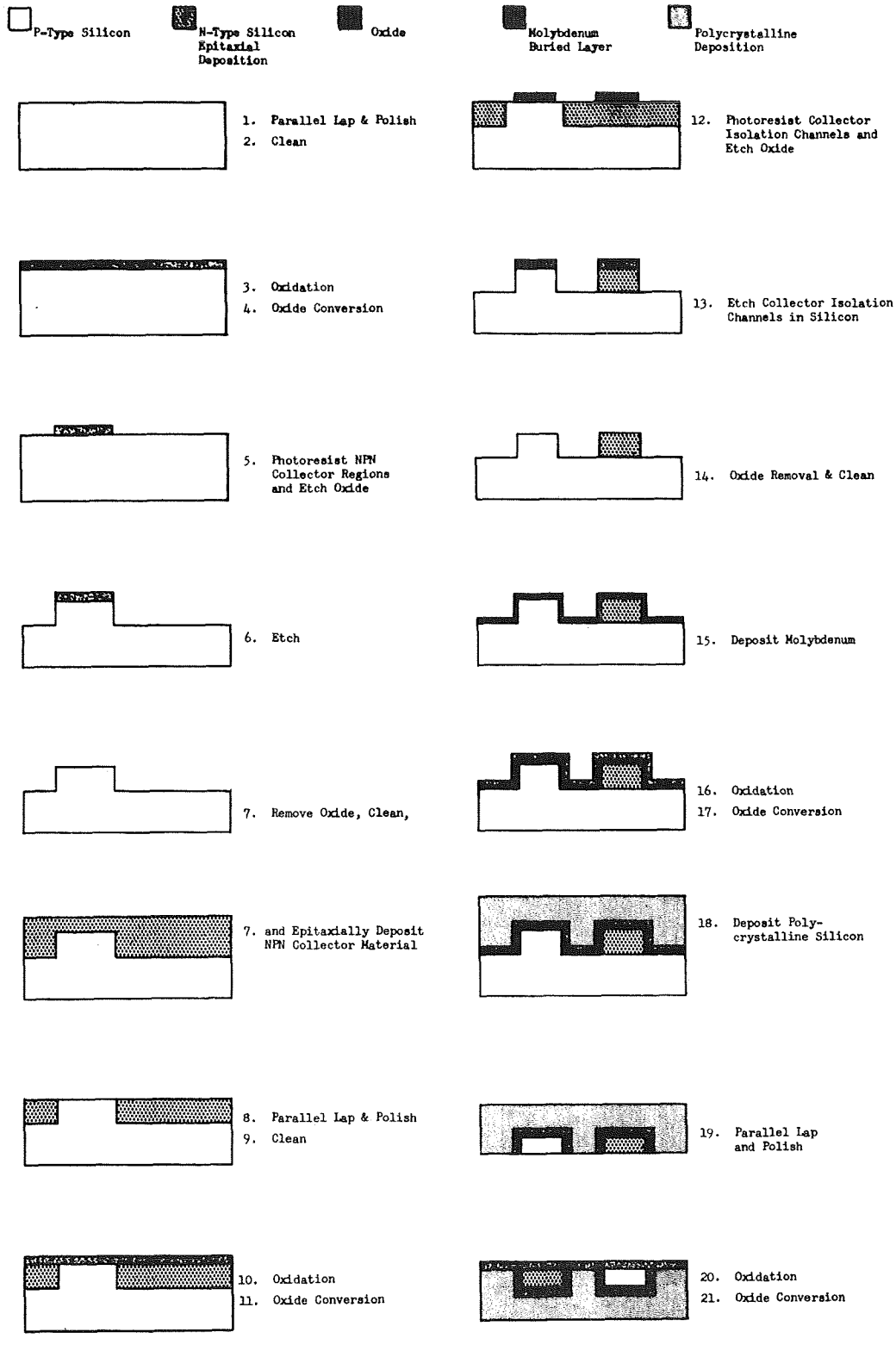

Figure A-2. MOA-5 Substrate Processing Steps

molybdenum layer to form isolated collector regions. An oxide passivation layer is grown and the wafer is ready for diffusions.

The diffusion processing steps are shown in Table A-4.

30. Start Diffusion - Add epi and P. Monitor wafers.

31. Silicon Etch - Method B. Ten parts HF, 10 parts H_2O_2, 80 parts H_2O. One minute etch at room temperature. DI rinse, methanol blow dry.

32. Clean - Method A_δ Three separate concentrated H_2SO_4 + 5% HNO_3 baths at 150°C, and one bath of concentrated HNO_3 at 150°C; 5 minutes in each bath. DI rinse and blow dry.

33. Thermal Oxide - 30 minutes at 1020°C wet O_2.

34. Ethyl Silicate - 750°C, 10,000Å.

35. Conversion - 20 minutes at 1020°C, dry O_2.

36. Photoresist - N base, Shipley.

37. Photoresist Clean - Method A.

38. Arsenic Deposition - 120 minutes at 1020°C. Remove oxide on P monitor wafer prior to run. 70 cc/min AsH_3 (1% in argon) 18 cc/min O_2, 7.5 cfh N_2.

39. Oxide Etch - Reduce oxide thickness to 1500Å ± 500Å. Read R_s. Desired = 450 ohms/square.

40. N Base Distribution - 180 minutes 1200°C; 3 parts: 1) 20 minutes O_2 2 cfh; 2) 85 minutes O_2 wet 80° on bubbler; 3) 75 minutes O_2 2 cfh. Read X_j.

41. Photoresist - P base, Shipley.

42. Photoresist Clean - Method A.

43. Boron Deposition - 30 minutes at 950°C. Remove oxide on epi monitor prior to run. 245 cc/min B_2H_6 (250 ppm B_2H_6 in argon); 80 cc/min O_2, 2450 cc/min N_2.

44. Oxide Etch - Reduce oxide thickness to 1500Å ± 500Å. Read R_s on epi monitor. Desired = 400 ohms/square.

45. Boron Distribution - 150 minutes at 1140°C; 2 cfh N_2 plus 4 cc/min O_2. Do last 15 minutes wet O_2. Read R_s and X_j on both monitor wafers. Desired epi = 210 at 2.6μ; P = 130 at 2.6μ. Recover monitor wafers with thermal oxide, 30 minutes at 1020°C wet O_2.

46. Ethyl Silicate - 750°C, 4000Å. All wafers.

47. Conversion - 15 minutes at 1020°C. Dry O_2.

48. Photoresist - N+ emitter, Shipley.

49. Clean - Method A.

50. N+ Deposition - _____ minutes at 1140°C, 150 cc/min Ph_3 (1% Ph_3 in argon). 50 cc/min O_2, 2.0 cfh N_2. Strip epi wafer before deposition.

51. Ethyl Silicate - 750°C, 4000Å. All wafers.

52. Conversion - 5 minutes at 1020°C dry O_2.

53. Photoresist - P+ emitter, Shipley.

54. Photoresist Clean - Method A.

55. P+ Deposition - 60 minutes at 1020°C. Remove oxide on P monitor prior to run. 200 cc/min B_2H_6 (1000 ppm B_2H_6 in argon). 30 cc/min O_2; 4.0 cfh N_2. Turn off B_2 after 45 minutes.

56. Oxide Etch - Etch to 1500Å. Read R_s + X_j on both N and P monitors. Desired R_s(P) = 12. R_s(N) = 5. X_j(P) = 1 and 2.6μ. X_j(N) = 1.5 and 2.6μ.

57. Ethyl Silicate - 750°C, 4000Å. All wafers.

58. Conversion - 20 minutes at 1020°C dry O_2.

59. Photoresist Contacts - Shipley. Remove oxide on back.

60. Clean - Method A.

61. Ethyl Silicate - 750°C, 4000Å. All wafers.

62. Conversion - 20 minutes at 1020°C dry O_2.

63. Photoresist Contacts - Shipley. Remove oxide on back.

64. Clean - Method A.

65. β Adjust

66. Metal I Deposition - TiAl.

67. Photoresist Cermet - Shipley

68. Metal Etch - TiAl.

69. Photoresist Removal - J-100.

70. Sinter - 30 minutes, 490°C.

71. Cermet Deposition -

72. Metal Etch -

73. Metal II Deposition - TiAl.

74. Photoresist Metal II - KTFR.

75. Metal II Etch - TiAl.

76. Photoresist Removal - J-100.

77. Sinter - 20 minutes, 450°C.

1/24/68

Table A-4. Diffusion/Surface Processing Sequence

Precision Thin-Film Cermet Resistors for Integrated Circuits

L. BRAUN AND D. E. LOOD

Abstract—The use of thin-film resistors in monolithic integrated circuits is becoming more widespread as the performance requirements imposed upon circuit designers become more stringent. A cermet, consisting of a mixture of Cr and SiO, was selected as a suitable resistor material for this purpose because of its compatibility with semiconductor materials and processes, and because of its stability and reproducibility over a wide range of sheet resistance. Cermet films with sheet resistances of 300, 1000, and 2000 Ω/square were flash evaporated on silicon substrates, and resistors were fabricated. The techniques for depositing the cermet films and fabricating the resistors are discussed, and methods for subsequently adjusting the resistors to precise values are described. The properties of the completed resistors are presented in detail.

Introduction

IT IS NOW widely accepted that the traditional methods of producing resistor elements for silicon monolithic integrated circuits are no longer adequate for many current applications [1]–[3]. Silicon resistors, including such categories as bulk silicon, diffused layers, epitaxial layers, and reverse-biased junctions, are now being replaced in critical designs with compatible thin-film resistors, which offer a wider range of values, increased precision, lower temperature coefficients, and greatly reduced parasitics. The use of thin-film resistors has made it possible for the first time to approach—and, indeed, in some cases to exceed—the performance obtainable with discrete components.

The chromium-silicon monoxide system has been favored by a number of investigators [4]–[6] as a thin-film resistor material because of its excellent stability, even for high sheet resistances. In addition, this cermet system (the term "cermet" designates a combination of a dielectric and a metal) appears especially compatible with the physical properties and processing requirements of monolithic integrated circuits.

This paper describes the procedures and techniques employed to fabricate compatible Cr-SiO cermet thin-film resistors. The precision, electrical characteristics, and stability will be discussed in detail.

Cermet Thin Films

Description of the Evaporation System

The cermet films are deposited by the flash evaporation [7] of mixed powders of SiO and Cr. The Cr powder is 99.95 percent, 325 mesh. The SiO powder is Kemet-select grade, 125–325 mesh. To insure complete mixing of the powders, the mixture is placed in a ball mill for at least 24 hours prior to its use in the powder hopper. Degassing of the mixed powder is accomplished by vacuum storage for at least 24 hours prior to deposition.

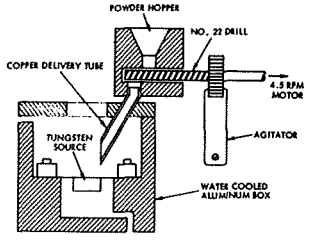

Fig. 1. Schematic of the flash evaporation source.

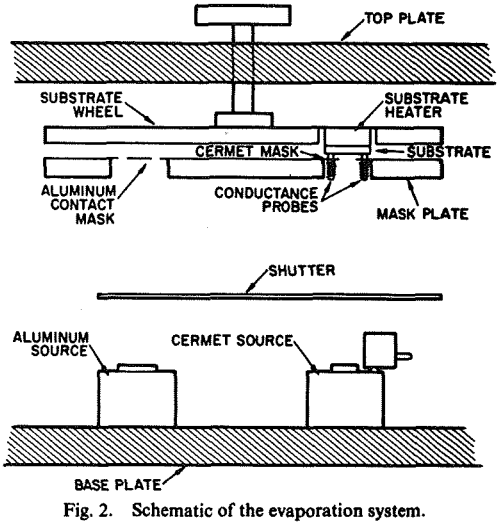

Fig. 2. Schematic of the evaporation system.

The evaporation source consists of a powder hopper, delivery tube, and a tungsten heater strip. The powder hopper has a horizontal worm screw below the powder reservoir that transports the powder to the delivery tube. The whole assembly is agitated by a gear and lever mechanism, as shown in Fig. 1. This continuous agitation prevents the powder from sticking in the delivery tube. The delivery tube directs the powder onto the tungsten strip, which is maintained at approximately 2000°C to insure instantaneous evaporation of both components. This mechanism is driven at 4.5 r/min, and gives a deposition rate of 4 to 4.5Å/s at a source-to-substrate distance of 9 inches.

The evaporation system is shown schematically in Fig. 2.

Manuscript received November 4, 1965; revised April 20, 1966, and July 14, 1966.

The authors are with the TRW Systems Group, TRW Incorporated, Redondo Beach, Calif.

Substrates are mounted on a copper block, which is heated by a number of tungsten coils imbedded in the copper. A gallium eutectic is used to insure good thermal contact between the copper block and the substrate. These substrate heaters will reach a maximum temperature of 500°C. Most of the depositions of cermet films have been at a substrate temperature of 400°C.

Early in the investigation it was found that these films would anneal; that is, the resistance would decrease if the films were heated to a temperature greater than or equal to their deposition temperature. In order that this material may be used as thin-film resistors in integrated circuits, it is important to use a substrate temperature that would not be exceeded in the processing steps necessary to complete the circuit after the deposition of the resistive film. A temperature of 400°C satisfies these requirements.

Thin-Film Deposition

Typically, the resistive film is simultaneously deposited on three substrates. One substrate is the silicon wafer on which the circuits are being fabricated. A second oxidized silicon wafer is used to monitor conductance. Both of these silicon wafers are on the same substrate heater. The third substrate is polished pyrex, on which the film thickness is later determined by multiple-beam interferometry. Periodically, films are also deposited on graphite substrates to permit spectrographic analysis of the film.

The procedure for the deposition of the cermet films is as follows. The system is usually pumped overnight so that, prior to the deposition, the pressure in the bell jar is 1×10^{-7} torr. Aluminum is deposited on one of the silicon substrates through a shadow mask to provide contacts for the conductance monitor. The substrates are then rotated over the mask used for the cermet deposition, and the conductance probes brought into contact with the monitor substrate. The substrates are heated to 400°C. The tungsten strip is heated to 2000°C, and the powder source is turned on and run for two minutes before the shutter between the source and substrates is opened. The pressure in the bell jar during the deposition is $2\text{–}3 \times 10^{-6}$ torr. The conductance of the film is monitored during the deposition and the shutter closed just short of the desired value. The final value of conductance is obtained by letting the film anneal at the deposition temperature until the conductance that corresponds to the desired sheet resistance (Ω/square) is reached. A conductance vs. time curve for a cermet deposition is shown in Fig. 3.

Resistivity of the Film

Initially, the deposition rate was monitored by means of a crystal oscillator thickness monitor; however, since the variations in rate were found to be very small, this was discontinued and the rate determined by dividing the film thickness by the deposition time. For each deposition, the conductance is monitored to its final value. Assuming that the rate remains constant, a linear conductance curve indicates that the conductance is directly proportional to the film thickness and that the deposited film is homogeneous.

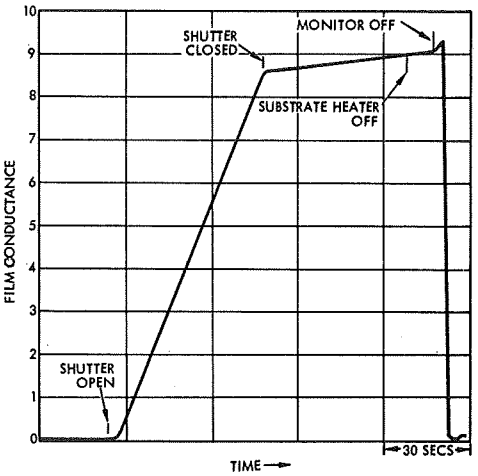

Fig. 3. Film conductance in arbitrary units as a function of time for a cermet deposition.

After the substrates are removed from the vacuum system, the resistance of the monitor is accurately measured with a Wheatstone bridge. The film thickness is measured with an interferometer and the resistivity of the material calculated. It is considered that the most important parameters to control, insofar as preservation of the electrical properties of the film is concerned, are the resistivity and the homogeneity. If the resistivity can be controlled to a reasonable degree, then the sheet resistance can be controlled much more precisely by slight variations in thickness.

The resistivity of cermet films with a nominal resistivity of 10^{-3} Ω-cm could be reproduced within ±10 percent. The sheet resistance of these films could be controlled to within ±5 percent. As the resistivity of the cermet films is increased, by the process of decreasing the chromium content, control becomes more difficult. Films with a nominal resistivity of 3.5×10^{-3} Ω-cm gave a ±20 percent variation in resistivity; however, it was possible to get reasonably straight conductance curves over this range. The apparatus used to monitor conductance is described in a previous publication [8].

Composition of Films

Spectrographic analysis of the evaporated films showed a large difference in the composition of the film, as compared with the composition of the mixed powder. As an example, films deposited from a mixed powder containing 69 percent Cr by weight were determined to contain 77 percent Cr by spectrographic analysis. This difference appears to be caused by the preferential bouncing of SiO particles. Visual observations indicate that when the SiO particles, which are larger and lighter than the Cr particles, hit the hot tungsten strip, the bottom surface vaporizes and the particle is propelled off the strip. This also happens to the Cr particles, but since they vaporize much slower and are more dense, the net effect is to lose much more SiO than Cr by this process. This argument is further substantiated by the fact that increasing the temperature of the tungsten strip decreases the re-

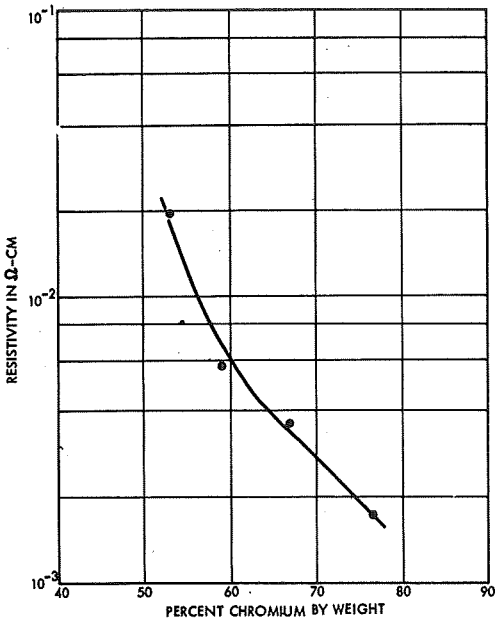

Fig. 4. Relationship between the cermet resistivity and the percentage of Cr in the film.

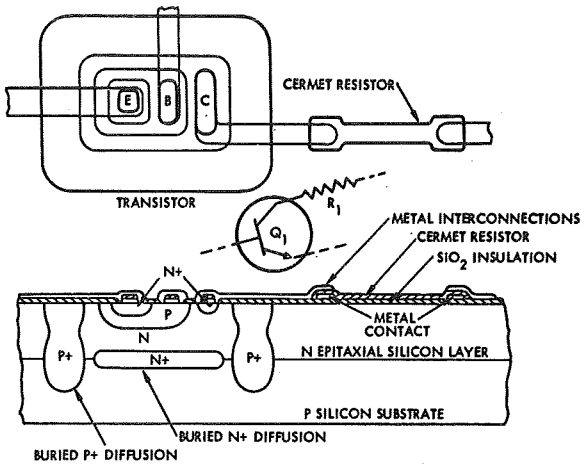

Fig. 5. Cross-sectional view of buried-layer epitaxial construction with deposited cermet resistor.

sistivity and the percentage of SiO in the film. Decreasing the source temperature has the inverse effect. The relationship between resistivity and percent Cr in the film, as determined by spectrographic analysis, is shown in Fig. 4. These results are similar to those reported by other authors for Cr-SiO cermet films [9], [10].

Resistor Fabrication

A typical cermet resistor entails a three-layer structure consisting of metal pads beneath the resistor terminations, the cermet resistive film, and finally the top metal contacts for connections between the resistor and other circuit elements. Figure 5 schematically depicts a portion of a silicon monolithic circuit, consisting of one transistor and a cermet collector resistor deposited upon the protective oxide. The cross-sectional view reveals that this particular circuit utilizes a buried-layer epitaxial construction; this, however, is only incidental to the resistor fabrication.

The initial resistor processing step is the deposition of the first metal. Approximately 600 Å of titanium followed by 5000 to 8000 Å of aluminum is vacuum deposited upon the oxide surface of the silicon substrate. Standard photolithographic techniques [11] are then employed to remove the metal in all areas—except for the resistor pads and over previously etched holes in the oxide, where it is necessary to make contact to the silicon substrate. A low-resistance, ohmic metal-to-silicon contact is obtained by alloying at 520°C.

Actually, were it not for the necessity of making contact to the silicon, the first metal could be eliminated. It is required because alloying cannot be accomplished after the cermet has been deposited since the cermet will anneal at temperatures much above its deposition temperature. This, presumably, could be circumvented by depositing the cermet at temperatures above 520°C; however, this has not yet been attempted because of limitations in the present equipment. The purpose of placing pads under the resistor terminations was to reduce contact resistance; however, comparative measurements have shown that their effect is negligible.

After completion of the first metal processing, the cermet film is deposited as detailed in the preceding section. Photolithography is again employed to delineate the resistors. The minimum practical resistor width is presently 0.5 mil; below this it becomes increasingly difficult to maintain dimensional tolerances. The maximum width, of course, depends on the available space, and in current applications is 15 mils. During the resistor etch procedure, the photoresist pattern also provides protection for the previously deposited substrate contacts. This is necessary since the cermet etching solution, which contains HF and HCl, readily attacks both titanium and aluminum.

The second vacuum-deposited metal layer, similar to the first, consists of 600 Å of titanium and 10 000 to 16 000 Å of aluminum. Photolithographic delineation produces the resistor contacts and, concomitantly, the circuit interconnections. Good electrical contact between metal and cermet is insured by sintering at 375°C in an inert atmosphere. At the sites where contact is made to the silicon substrate, continuity between top and bottom metal is interrupted by the layer of cermet that was left to protect the bottom metal from the cermet etch. This film is thin enough, however, that the series resistance it introduces is negligible.

Characteristics of Cermet Resistors

Three variations of the cermet films were used in fabricating resistors. Designated as Type I, II, and III, they were characterized by sheet resistances of 300, 1000, and 2000 Ω/square, respectively. A summary of their properties is presented in Table I.

In typical circuit applications, the limitations on line

TABLE I

PROPERTIES OF CERMET FILMS

	Type I	Type II	Type III
Sheet resistance (Ω/square)	300	1000	2000
Specific resistivity (Ω-cm)	10^{-3}	3×10^{-3}	3×10^{-3}
Film thickness (Å)	300	300	150
Chromium content (% by wt.)	77	66	66
Temperature coefficient (ppm/°C)	$+140\pm50$	-125 ± 50	-125 ± 50
Power dissipation at burnout (W/in^2)	2.9×10^5	2.4×10^5	2.2×10^5

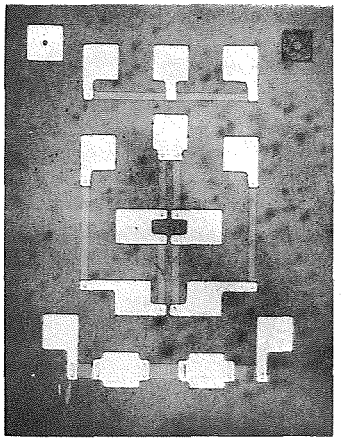

Fig. 6. Resistor test pattern. The bottom metal pads (the small dots at the resistor terminations) are visible through the top metal and cermet.

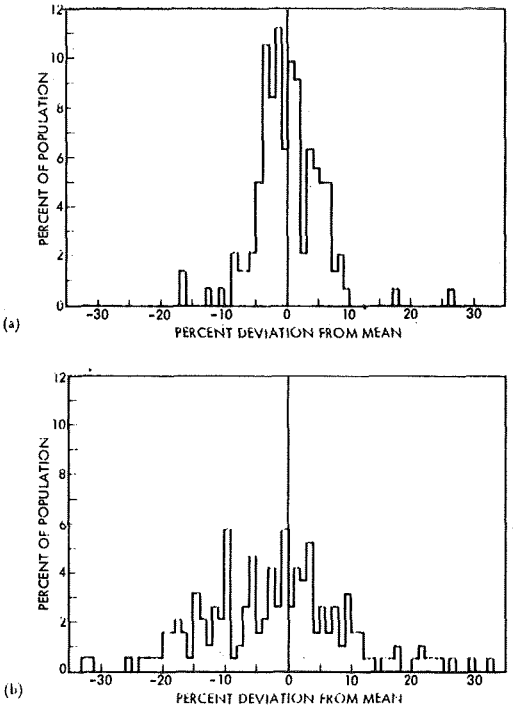

Fig. 7. (a) Distribution of 1 mil wide cermet resistors (b) Distribution of 1-mil wide diffused silicon resistors.

width and available space have permitted resistance values ranging from 150 to 200 000 Ω using 300 Ω/square cermet. With 2000 Ω/square films, the upper bound has been extended to 1.3 MΩ.

For test purposes, resistor patterns of the type shown in Fig. 6 were prepared. The substrates were identical to those used for circuit fabrication, except that there were no prior diffusions. The resistors could thus be examined independently of any subsurface components.

Precision

Integrated circuit resistors, by virtue of their simultaneous fabrication, display a high degree of uniformity. To take advantage of this characteristic, integrated circuits are designed, whenever possible, to depend upon resistor ratios for their performance rather than absolute values.

For identical, adjacent, 1-mil wide resistors, the average deviation in resistance is ±0.6 percent. The equivalent value for 0.5-mil wide resistors is ±1.1 percent. For nonadjacent resistors on a typical 60-mil square circuit chip, the deviation averages ±1.8 percent for 1-mil wide resistors and ±2.5 percent for 0.5-mil wide resistors. Only a slight improvement is noted for resistor widths greater than 1 mil.

The absolute values of 1-mil wide resistors are normally within ±15 percent of the design value. About half of this amount is due to resistivity and thickness variations introduced during the film deposition, while the remainder can be ascribed to variations in resistor dimensions as a result of the photoresist and etching process. The histogram of Fig. 7(a) shows a typical distribution of 1-mil wide cermet resistors on a 1-inch diameter silicon substrate. An interesting comparison is offered by Fig. 7(b) which shows the distribution previously attained using diffused resistors.

Resistor Adjustment

Thin-film resistors have yet another advantage over silicon resistors—the ability to adjust the resistors to a precise value after fabrication. This not only allows the use of resistors with tighter tolerances than those otherwise available, but also permits compensation of other components in the completed circuit, a function associated with potentiometers or trimming resistors in conventional circuitry.

Two adjustment techniques have been used successfully with cermet resistors. The first is a resistor array with removable shunts, and the second is an electrical pulsing technique.

The first technique utilizes a resistor network, such as the one shown in Figs. 8(a) and 8(b). Certain of the resistors are shunted by deposited metal links; these may be removed by passing current through the links and evaporating them, as shown in Figs. 8(c) and 8(d). Removing the coarse-adjustment links, on the left-hand side of the schematic in Fig. 8(a), adds series resistance in a binary fashion, with 150 Ω as the smallest increment. Removing the fine-adjustment links, shown on the right-hand side of the schematic, adds

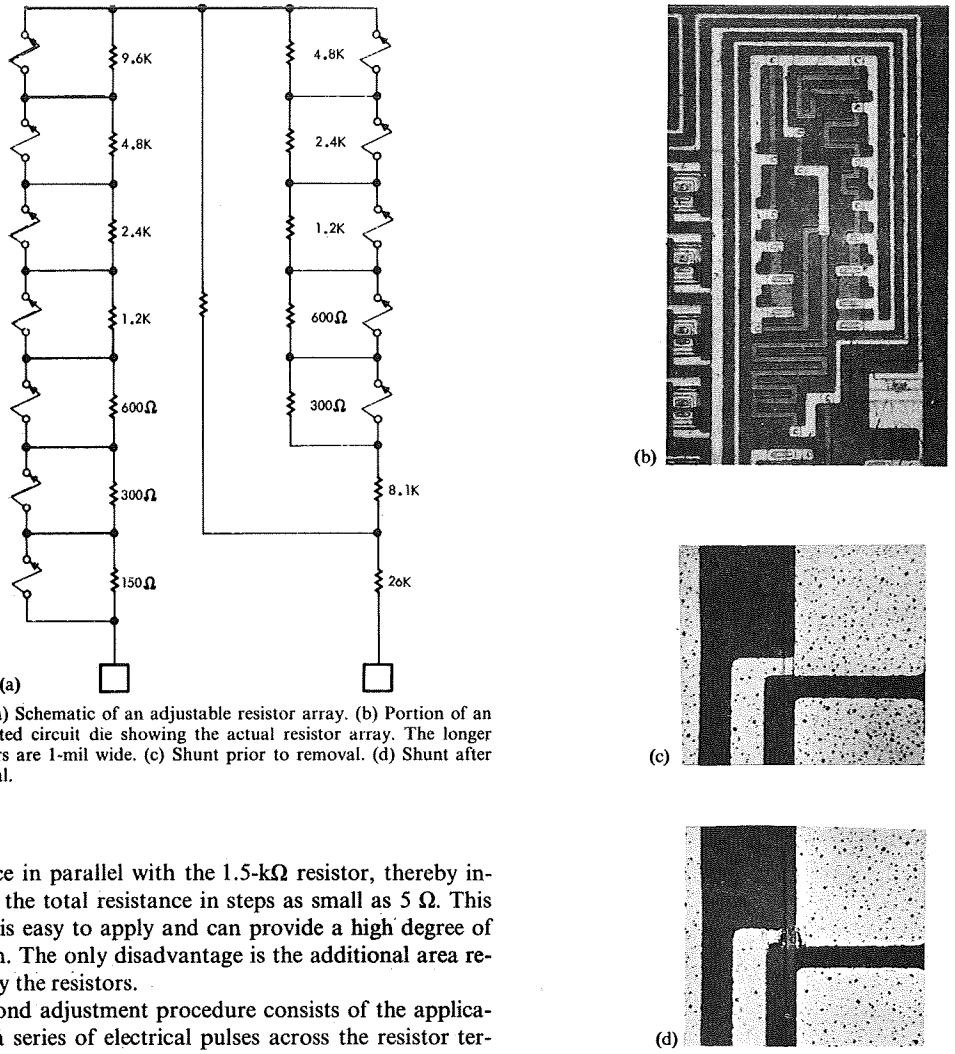

Fig. 8. (a) Schematic of an adjustable resistor array. (b) Portion of an integrated circuit die showing the actual resistor array. The longer resistors are 1-mil wide. (c) Shunt prior to removal. (d) Shunt after removal.

resistance in parallel with the 1.5-kΩ resistor, thereby increasing the total resistance in steps as small as 5 Ω. This method is easy to apply and can provide a high degree of precision. The only disadvantage is the additional area required by the resistors.

A second adjustment procedure consists of the application of a series of electrical pulses across the resistor terminals, while simultaneously monitoring the resistance. For pulses producing a peak power dissipation of approximately 10^6 W/in^2 of resistor surface, the resistance exhibits a steady decrease. When the desired resistance is reached, pulsing is halted and the resistor will remain at this new value. In this way, adjustment to better than ± 0.1 percent has been readily achieved.

The source of this behavior is believed to be an annealing process arising from the momentary high temperature produced by each electrical pulse. Electron microscope studies have revealed that the annealing process in these films produces a structural change in the direction of increased ordering.

Although this method has been used with considerable success in fabricating a number of circuits, it does have several drawbacks. First, it is necessary to remove the resistor from the circuit during the adjustment procedure to avoid damaging or altering other components. This is accomplished by providing removable links similar to those employed in the first method. After the adjustment is completed, the resistor is connected back into the circuit by bridging the open section with a thermocompression ball bond.

There is also a limitation on the maximum value of resistance that can be adjusted. If the pulse amplitude required for adjustment is too high, breakdown of the insulating oxide layer between the resistor and the silicon substrate can occur.

Finally, for reasons not yet understood, some resistors do not change in a fully controllable manner, but instead display a series of discrete and sometimes large step changes.

Presently under investigation is a potentially superior technique that would replace electrical pulses for heating the resistors with high-energy light pulses from a laser source. This method would not require physical contact with the circuit and may also eliminate the difficulties now associated with the electrical pulse technique.

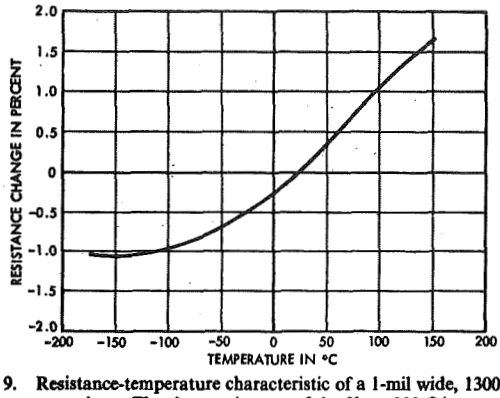

Fig. 9. Resistance-temperature characteristic of a 1-mil wide, 1300-ohm cermet resistor. The sheet resistance of the film = 300 Ω/square.

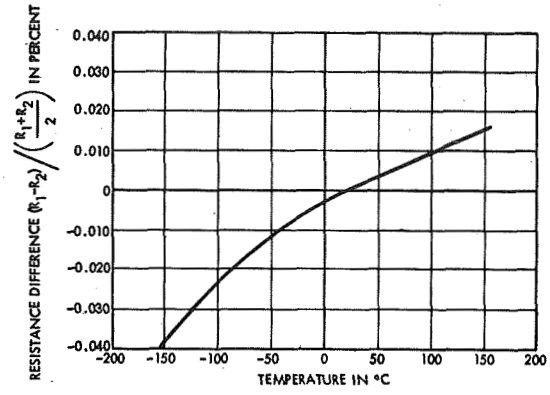

Fig. 10. Tracking characteristic of two adjacent 1-mil wide, 1800-ohm cermet resistors. The sheet resistance of the film = 300 Ω/square.

Temperature Coefficient of Resistance

The average temperature coefficient between −25°C and +100°C is 140±50 ppm/°C for Type I cermet ($\rho = 10^{-3}$ Ω-cm) and −125±50 ppm/°C for Types II and III cermet ($\rho = 3 \times 10^{-3}$ Ω-cm). A typical resistance-temperature curve for a Type I cermet resistor is shown in Fig. 9.

More important than the temperature coefficient in many applications is the tracking coefficient; i.e., the deviation in the ratio of two resistors as a function of temperature. The outstanding performance of cermet resistors in this area is clearly demonstrated in Fig. 10. For the example shown, the tracking coefficient is better than ±1 ppm/°C from −150°C to +150°C.

Stability

An intensive test program is now in progress to determine the stability and reliability of cermet resistors. Preliminary results on resistors using 300 Ω/square cermet support previous conclusions concerning their stability.

Partial results of temperature storage tests are shown in Fig. 11. The drift rate at 200°C is 1 percent per 1000 hours, and at 150°C is 0.25 percent per 1000 hours. The direction of the resistance change is positive, and here the mechanism is believed to be oxidation of the chromium. If this is actually the case, then a protective coating of some material, such as SiO, should result in a still lower drift rate.

Cermet resistors also demonstrated excellent resistance to moisture. Unprotected resistors were directly exposed to an environment of 60°C and 95 percent relative humidity. No significant changes were noted after 500 hours.

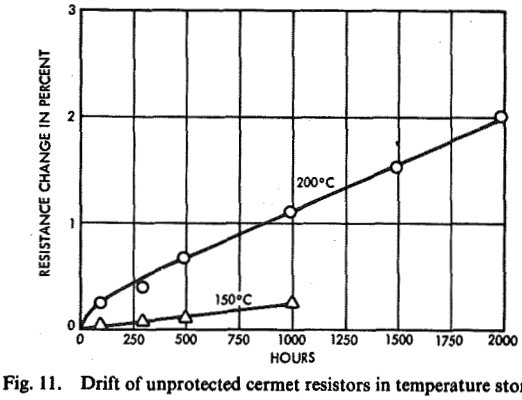

Fig. 11. Drift of unprotected cermet resistors in temperature storage.

Power Dissipation

To obtain information on the power-handling capabilities of the three types of cermet films, burnout tests were performed on individual rectangular resistors, measuring 1 mil by 6 mils, which were deposited on thermally oxidized silicon wafers of both chemically polished single-crystal material and mechanically polished polycrystalline material. For either substrate, the average power dissipation at burnout was 1.7 W (2.9×10^5 W/in^2) for Type I cermet, 1.4 W (2.4×10^5 W/in^2) for Type II cermet, and 1.3 W (2.2×10^5 W/in^2) for Type III cermet. These figures suggest that the burnout power is a function of the film resistivity and, to a lesser degree, the thickness.

There are other factors, of course, that also affect the maximum power dissipation. In an actual circuit, it would be necessary to consider the effects of different resistor geometries (e.g., meandered resistors vs. linear resistors), the dissipation and proximity of other resistors in the circuit, and the thermal properties of the packaging employed. A quantitative assessment of these factors has not yet been obtained; however, based on preliminary load life tests on various test patterns, 10^4 W/in^2 in a 25°C ambient has been established as the maximum permissible dissipation for design purposes. In circuit applications thus far, the highest dissipation utilized has been 6×10^2 W/in^2. For 1-mil wide, 300 Ω/square resistors, this corresponds to 2 mW/kΩ of resistance.

Applications

Cermet thin-film resistors have now been applied successfully in a number of integrated circuit designs. Notable among these is a recently described [12] high-frequency dc amplifier of exceptional performance. This amplifier features a bandwidth of 60 to 90 MHz, a differential gain of 70, and a power dissipation of 45 mW.

An earlier version of this circuit had previously been fabricated using triple-diffused transistors and diffused resistors. The updated circuit employs buried-layer epitaxial construction and cermet resistors, which are adjusted to precise values after deposition. Performance is markedly improved in the later version, and a significant portion of this improvement is directly attributable to the use of the cermet resistors, which provide the necessary features of high precision, low temperature coefficients, excellent tracking, and reduced parasitic capacitance. Of no less importance is the additional design flexibility provided by a wider range of available resistance values and by increased processing freedom; since the resistors and semiconductors are fabricated in separate and independent processes, it is no longer necessary to compromise the characteristics of one type of component to meet the requirements of the other.

Conclusions

Evaporated Cr-SiO cermet films appear to be an excellent choice for use as resistor elements in silicon monolithic integrated circuits. Cermet resistors are readily adaptable to integrated circuit processing and possess excellent electrical and physical characteristics. High precision can be provided by techniques that permit adjustment of the resistors after fabrication. In addition, films with sheet resistances of 2000 Ω/square make possible the use of large values of resistance. The continuing investigations of cermet films will be directed toward developing reproducible films of still higher resistivity, which will be required for further advances in the design of micropower circuitry.

Acknowledgment

The authors wish to express their appreciation to Dr. J. L. Rogers and J. L. Buie for their encouragement and helpful comments, to L. Rosenkrantz who deposited many of the films, and to W. B. Adelman who supplied the stability data.

References

[1] E. R. Dean, "The intermarriage of silicon integrated circuits and thin film passive components," *1964 Proc. IEEE 3rd Annual Microelectronics Symp.*
[2] I. A. Lesk, "Thin film hybrid techniques," *Solid State Design*, vol. 5, pp. 38–41, July 1964.
[3] R. M. Burger and R. P. Donovan, "A broader choice of components for silicon integrated circuits," *Electronics*, vol. 38, pp. 48–59, May 1965.
[4] M. Beckerman and R. L. Bullard, "Integrally fabricated resistors and their performance," *1962 Proc. Electronic Components Conf.*, pp. 53–56.
[5] F. S. Maddocks, "Recent progress in the fabrication of film circuit panels," presented at the IEEE 3rd Annual Microelectronics Symp., St. Louis, Mo., 1964.
[6] R. Wagner and K. M. Merz, "Stable high range, Cr/SiO film resistors," *1964 Proc. Electronic Components Conf.*, pp. 97–106.
[7] L. Harris and B. M. Siegel, "A method for the evaporation of alloys," *J. Appl. Phys.*, vol. 19, pp. 739–741, August 1948.
[8] A. J. Learn and R. S. Spriggs, "Behavior of film conductance during vacuum deposition," *J. Appl. Phys.*, vol. 34, pp. 3012–3021, October 1963.
[9] W. J. Ostrander and C. W. Lewis, "Electrical properties of metal-dielectric films," *Trans. Eighth Symp. Am. Vacuum Soc.*, vol. II. New York: Pergamon, 1962, pp. 881–888.
[10] M. Beckerman and R. E. Thun, "The electrical and structural properties of dielectric metal mixtures," *ibid.*, pp. 905–971.
[11] "Kodak Photosensitive Resists for Industry," Eastman Kodak Co., Rochester, N.Y., publication P-7, 1964.
[12] D. R. Breuer, "Integrated high-frequency D.C. amplifiers," presented at the 1964 WESCON Conf., Los Angeles, Calif.

Reprinted from the PROCEEDINGS OF THE IEEE
VOL 54, NO. 11, NOVEMBER, 1966
pp. 1521-1527